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Implementation of energy-efficient low-power CMOS 4:2 compressor using DG FinFET technique

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Abstract

The Double-Gate FinFET technique is proposed in this work for the implementation of a CMOS 4:2 compressor. The main objective of this study is to reduce leakage power and leakage current while maintaining comparable performance with fewer transistors. This paper presents a high-performance CMOS 4:2 compressor based on an optimized logic architecture. The proposed Double-Gate FinFET approach reduces process variation effects in CMOS 4:2 compressor circuits, mainly by decreasing leakage power and delay. Double-Gate FinFET technology is suitable for logic cells because it provides improved speed, lower threshold-voltage operation, reduced leakage, and enhanced performance. The proposed CMOS 4:2 compressor design was simulated using Cadence Virtuoso at 90 nm technology.

Keywords: CMOS; 4:2 Compressor; Leakage Power; Power Delay Product; Delay; Cadence Virtuoso; DG-FinFET

1. Introduction

The usage of arithmetic circuits in portable devices has grown in popularity in recent years. Electronic equipment like mobile phones and digital signal processors (DSPs) have been attempting to lower the amount of energy they use [1], [2]. Cells with low power consumption and good performance are explored; however, it is challenging to optimize circuit characteristics concurrently in an integrated circuit (IC) [3], [4]. As a result, various trade-offs must be made in the design of computational circuits. Increases in signal processing speed are often accompanied by increases in power usage. Compilers, multipliers, subtractors, and comparators are significant arithmetic circuit types, all of which use full adders (FAs) as structural elements [5], [6]. Because successful signal processing requires qualified FA cells in DSP blocks, it is crucial to design an FA circuit that carefully balances important factors like power and latency. Instead of optimizing all three characteristics at once, designers tend to focus on only one [7]. The designers are more concerned with power consumption reduction than delay. Because of this, academics have been working on new strategies to decrease power, for example, by integrating new designs and technologies [8]. For image processing filters and speeding up motion estimates, low-power fast FAs may be used in digital compressors [9]. There were three-, four-, five-, and seven-compressors offered by circuit designers; however, the most common variants for rapid computational ICs are the four- and five-compressors [9], [10]. The DG FINFET technique has been used to reduce the space and output swing cost of 4:2 compressors in recent years, as have alternative gate- and transistor-level topologies in chip designing [11].

Historically, the multiplier has been used to simplify arithmetic circuits by performing three functions: partial product reduction, partial product creation, and addition. As the use of multimedia devices grows, so does the need to properly organize the power and voltage sources [12]. As far as chip design is concerned, multipliers and adders are the most common power guzzlers. It is common for lower-order compressors like 3:2 and 4:2 compressors to be utilized as standard components in many digital signal processing (DSP) applications [13]. 4:2 compressors have been developed in this work employing a variety of logic types in conjunction with the CMOS logic that is already there [10], [14]. In this

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proposed 4:2 compressor architecture we can design by using a smaller number of transistors for implementation. We perform the compressor design by using conventional logic styles, which are discussed using these low-power adder architectures. To decrease the amount of electricity dissipated, we may lower the supply voltage. By lowering the number of transistors, we may minimize and simplify the complexity of circuits in both arithmetic and digital systems by using this strategy. Compressors are employed in multiplier circuits to minimize power consumption and delay because of their ability to simplify complicated calculations. Today, 4:2 and 5:2 compressors are frequently used for high-speed and high-performance multipliers because of the decreased response time of the partial product accumulation step. In terms of the structure of regular construction of a Wallace tree with less complexity, the 4:2 compressor is the only one. It has been suggested that different 4:2 compressor circuits may be used to reduce power consumption and maximize space efficiency. As CMOS architectures need a large number of transistors to work at low supply voltage levels, some of them can function at low voltages but require a huge amount, while others are less efficient and cannot drive the next level of the systems.

2. 4-2 Compressor

Using a 4:2 compressor, you can get two half products out of four whole ones. Fig. 1 depicts a block diagram of a 4-2-1 compressor (a). Cin and M1 are the only two required inputs, whereas Sum, Carry, and Cout are the only three required outputs. There are two compressors, one in the previous lower significant stage, and one in the next higher significant stage, each with different input and output. Cin and Sum have weights that are similar to those of M1, 2, 3, and 4, but Carry has a binary bit order that is one higher, at i+1. Compressors are preferable to complete adders due to fact that Cout is independent of Cin. Fig. 1 shows 4:2 compressors with 2 serially linked full adders (b). Four XOR gates provide a critical route delay in this implementation. The following equation must be followed while designing a 4-2-1 compressor:

$$M_1 + M_2 + M_3 + M_4 + C_{in} = Sum + 2 * (Carry + C_{out})$$

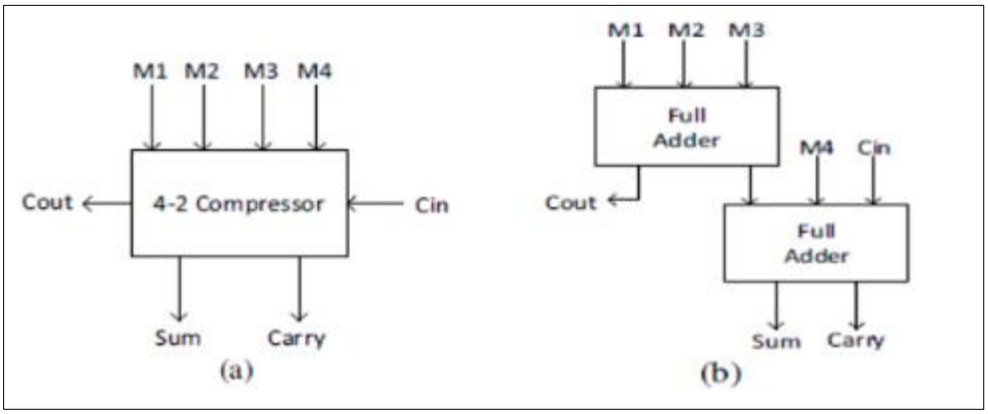

Figure 1 (a) Block diagram and (b) full-adder-based configuration of a 4:2 compressor

The 4:2 compressor has been implemented in a variety of ways in the literature .Fig 2. Depicts two popular designs for 4:2 compressors. XOR gates and multiplexers are used in the first one (MUX). Three XOR gates make up the critical route delay. Later on, the design of the first one has been changed to include XOR-XNOR modules and MUXes. XOR-XNOR module and two MUXs add crucial route delay to the circuit. The following equations provide the basis for implementing these architectures:

$$Sum = M_1 \oplus M_2 \oplus M_3 \oplus M_4 \oplus C_{IN} \quad (1)$$

$$C_{out} = (M_1 \oplus M_2) * M_3 + \overline{M_1 \oplus M_2} * M_1 \quad (2)$$

$$Carry = (M_1 \oplus M_2 \oplus M_3 \oplus M_4) * C_{IN} + \overline{M_1 \oplus M_2 \oplus M_3 \oplus M_4} * M_4 \quad (3)$$

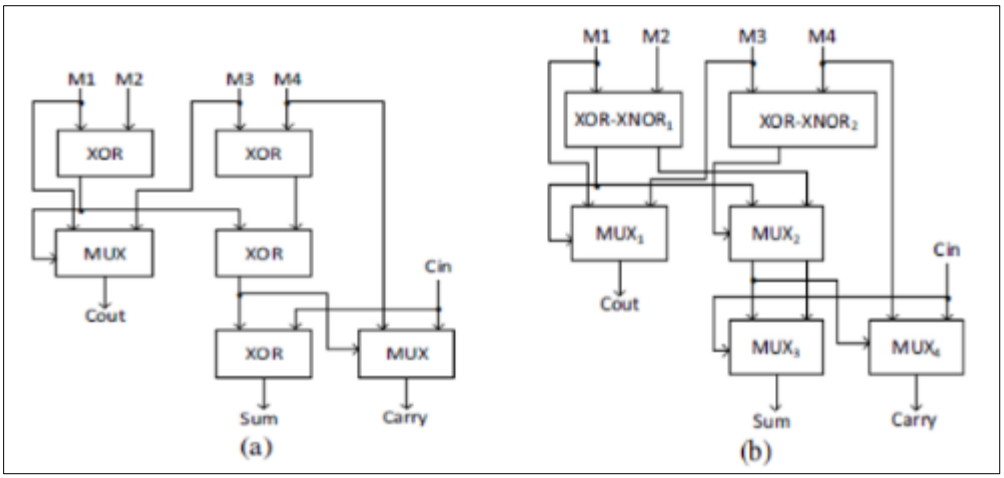

Figure 2 (a) Block diagram using XOR logic style and (b) block diagram using XOR-XNOR logic style

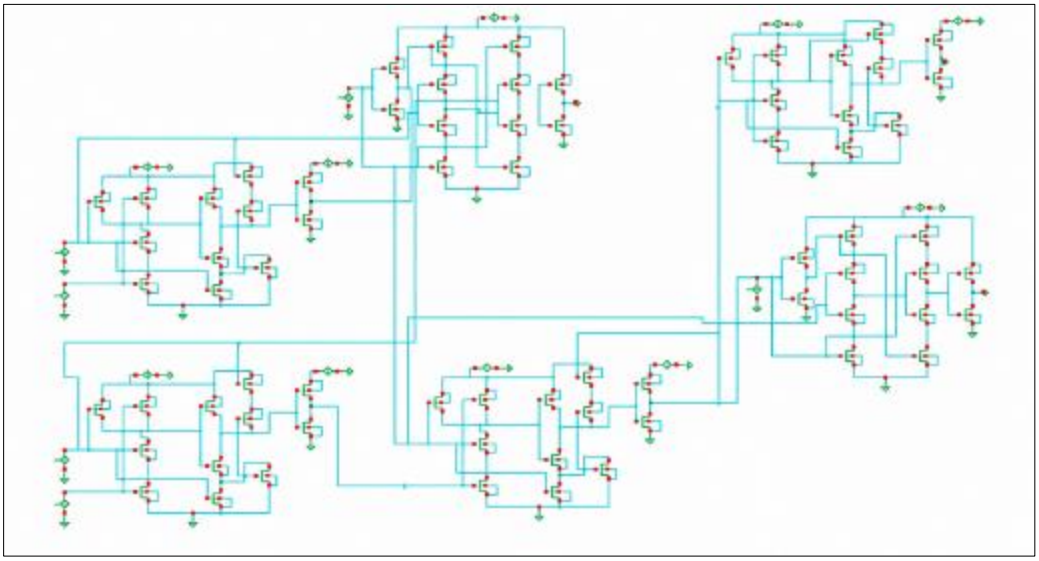

Figure 3 Schematic of a CMOS 4:2 compressor

Fig. 3 depicts a four-to-two compressor built on CMOS logic. As the number of transistors increases [19], [13], so does the power consumption, area covered, and delay time. Chang et al. (2004) present 4:2 compressors built entirely on DPL (Double Pass-Transistor Logic). The original architecture was used to construct this high-speed compressor. DPL XOR-XNOR modules, which concurrently produce XOR and XNOR signals, are replacing XOR gates. Select and complement inputs of the multiplexer are connected to XNOR and XOR signals, respectively. Because of this, certain multiplexer inputs no longer need an inverter. Because of the necessity for input inverters, DPL XOR-XNOR modules increase switching activity, which results in a compressor that uses more power.

Fig. 2(b) shows the architecture utilized in [19], which employs CMOS logic for XOR-XNOR1 and XNOR2 modules, as well as MUX1,3,4. The compressor's speed is increased because of the gate logic approach utilized in MUX2 transmission. As MUXs do not need an additional converter for select inputs, the power consumption is likewise reduced.

Tonfat and Reis (2012) [13] show the 4:2 compressor that makes use of the transmission version of MUX and a 10T XOR-XNOR module. Because of the MUX's inverters, power consumption is higher. In the next step, the available XNOR and XOR signals are not correctly exploited. As suggested in Kumar and Kumar (2014) [18], an improved 4:2 compressor by an 8T XOR-XNOR module consumes less power. Because fewer transistors are utilized, the compressor takes up less space.

3. Proposed Novel CMOS 4:2 Compressor

A novel 4:2 compressor architecture using transmission gate logic and two 8T XOR-XNOR modules and 4 MUXs. According to Tonfat and Reis (2012), an entirely new 6T XNOR gate has been suggested. High speed and complete output voltage swing are provided by this XNOR gate, but it also uses less power. An inverter must be connected to the XNOR gate's output for XOR functionality. As a result, the XOR-XNOR module in Figure 4 utilizes a total of eight transistors (a).

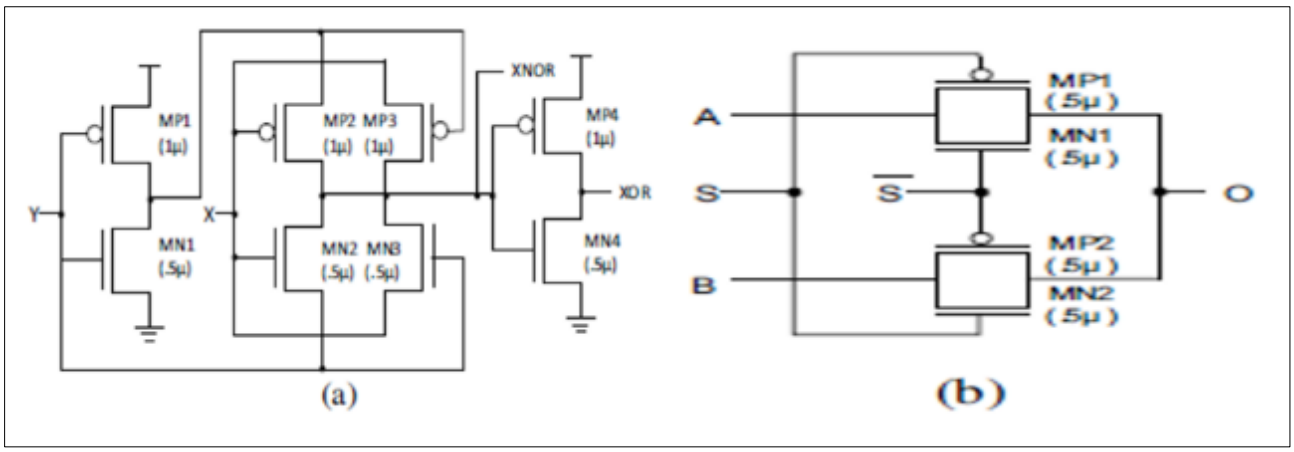

Figure 4 (a) Eight-transistor XOR-XNOR logic style and (b) transmission-gate-logic-based MUX

Complement of input Y is generated by an inverter comprising MN1 and MP1 transistors in this XOR-XNOR module. Using two transistors, MN2 and MP2, this inverter controls the output of the second inverter. There is a problem with voltage degradation when using this 2nd inverter to simulate XNOR function for X and Y inputs for X=0, Y=1 and X=Y=1 (Chang, Gu and Zhang, 2004). To circumvent this issue, 2-level restoring pass transistors MN3 and MP3 are utilized. Because this module's inputs X=Y=0 turn on transistors MP1 and MP2, the output is logic high (XNOR). By applying logic low to the output node, which is connected to a transistor MP3, transistors MP2, MP3, MN1, and MN3 are turned on. Inputs X=1 and Y=0 turn on transistors MP1 and MN2, as well as output node, illustrates logic low. A logic high level is achieved by turning on all three transistors MP3, MN1, and MN2 when the inputs X=Y=1. Transmission gate logic is utilized to create the MUX depicted in Figure 4 (b). An inverter is used solely by the Sum generator (MUX3) when generating a signal that is the inverse of the select input it receives. Cout generator (MUX1) and MUX2 select inputs are supplied from the XOR-XNOR modules' outputs. The Carry generator is also connected to MUX2's output and its complement form (MUX4). Having removed inverters, the compressor's critical path latency and the number of transistors required to operate it have been reduced. Transmission gate logic type MUX transistors of the same size are used to increase the compressor's speed and reduce power consumption, respectively, in the inverter. There are transistor widths shown inside the brackets in Fig. 4. Fig. 5 depicts the new planned 4:2 compressor's entire circuit design.

The proposed architecture uses transmission-gate-based multiplexers to improve switching performance and reduce delay. Since the select and complementary select signals are directly available from the XOR-XNOR modules, the number of extra inverters is reduced. This helps in minimizing the transistor count, power dissipation, and critical path delay.

The proposed compressor uses fewer transistors compared with the conventional CMOS 4:2 compressor. As a result, the circuit becomes more compact and power efficient while maintaining proper output voltage swing and functionality.

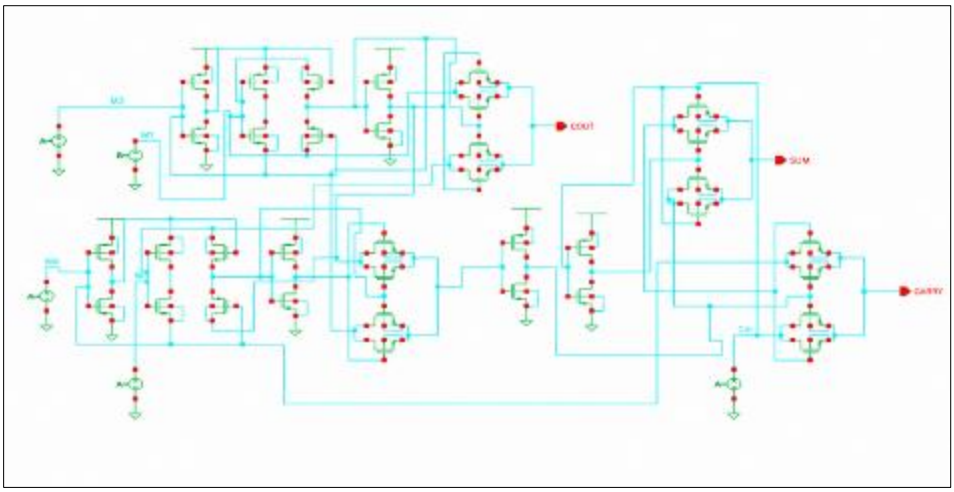

Figure 5 Suggested schematic of the new CMOS 4:2 compressor

4. CMOS 4:2 Compressor Using DG FinFET Technique

Fin Field Effect Transistor (FinFET) is the abbreviation. FinFET is a non-planar dual-gate transistor used in silicon architecture that offers a high computational density. The FinFET is one of the most important new multigate devices due to its simplicity of manufacture and excellent compatibility with planar MOSFETs. FinFET devices have greater on-state current, lower off-state current, and faster switching rates due to the enhanced control of their conductive channel provided by their double gate. There are three operating modes for FinFET circuits: SG (Shorted Gate), LP (Low Power), and Independent Gate (IG). Fig. 6 depicts the FinFET model's three-dimensional structure (a) and top cross-section (b). Some studies say that this tendency has persisted, while others argue that beyond 65 nm, this is no longer the case. Various modes of operation have diverse features, allowing for more design freedom. A high on-state current and rapid switching speed are advantages of the SG-mode FinFET, whereas a low off-state current and reduced leakage power dissipation are advantages of the LP-mode FinFET, respectively.

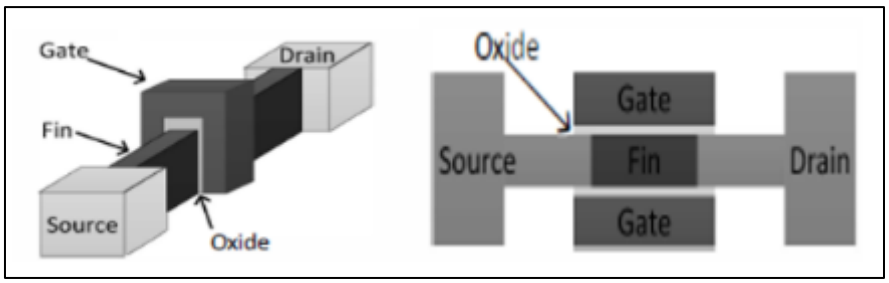

Figure 6 FinFET model: (a) 3-D structure and (b) top cross-sectional view

The 4:2 compressor is implemented using a double-gate FINFET. DG FINFET's front and rear gates may be utilized to generate execution and reduce control use thanks to the self-determining control of these two gates. To integrate parallel transistors in non-basic ways, self-deciding gate control may be used. It is not a surprise that Double-Gate (DG) FINFETs have been designed to manage short channel effects and regulate leakage current. The second gate is added inverse to the typical gate.

FINFET's four modes of operation are referred to as short gate, independent gate, low power and ideal power, and crossover mode. Continuous scaling down of bulk CMOS is problematic due to the material it is made of. Issues in the 45 nm scaling of mainstream CMOS include short channel effects, optimal current, gate-dielectric leakage and the variety of devices in a given family. Instead of scaling inhibitors, FINFET-based devices at 45 nm enable better control over short channel effects with lower leakage. The schematic of the 4:2 compressor utilizing the Double Gate FINFET (DG FINFET) technique is seen in Fig. 7.

In the proposed work, the CMOS 4:2 compressor is implemented using the DG-FinFET technique to reduce power dissipation and delay while maintaining correct logic operation.

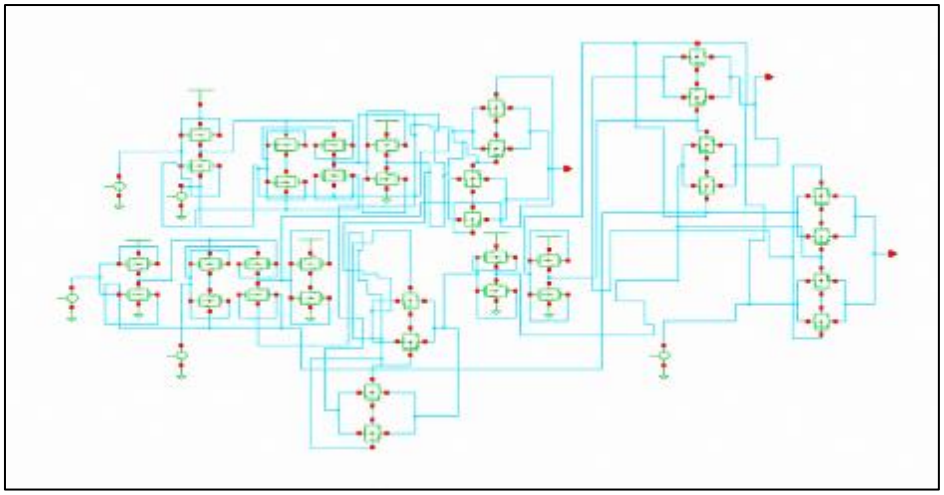

Figure 7 Schematic diagram of the new CMOS 4:2 compressor employing the DG FinFET method

5. Simulation Results and Performance Analysis of the Proposed Novel CMOS 4:2 Compressor

Cadence Virtuoso Tool is used to perform the simulations in 90 nm CMOS technology. Table 1 lists the suggested compressor's performance characteristics for supply voltages ranging from 0.7 V. There is a correlation between the greatest delay in the output, the average power usage, as well as PDP. Compressor transient response is seen in Fig. 8.

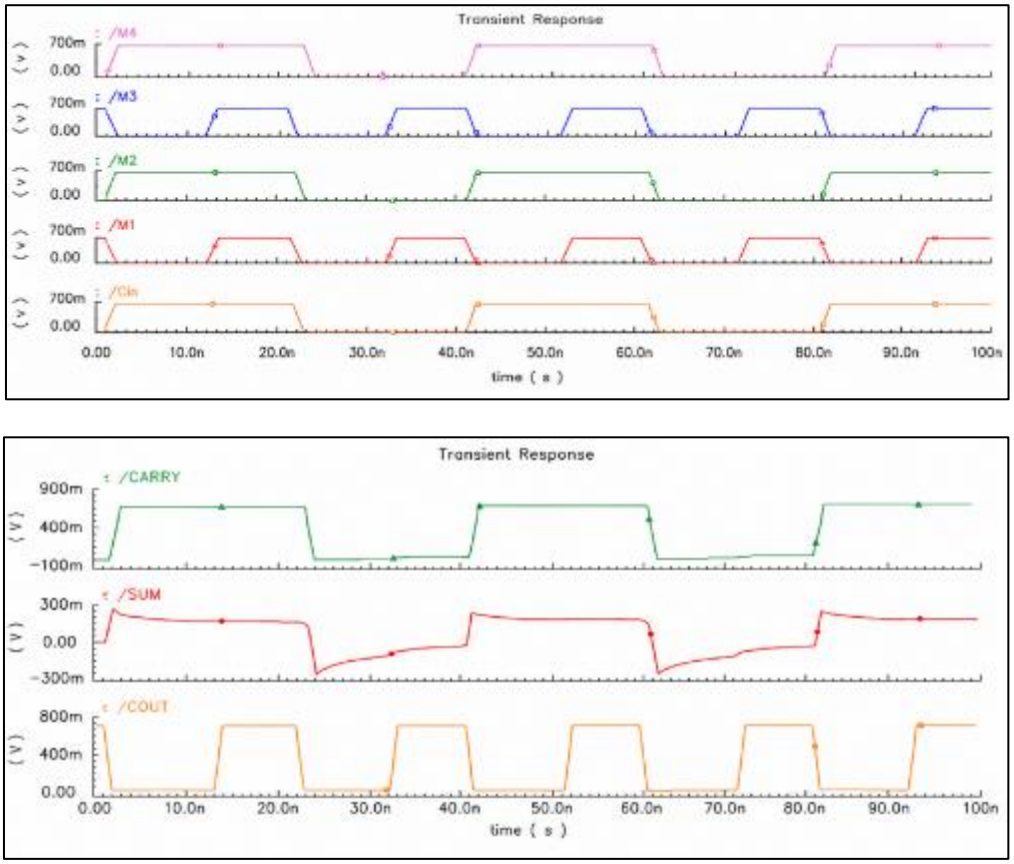

Figure 8 Transient response of the suggested CMOS 4:2 compressor

The Cadence tool has been used to simulate the proposed CMOS 4:2 compressor circuit utilizing 90 nm technology and a nominal supply voltage of 0.7 V. To reduce power consumption while preserving CMOS 4:2 compressor circuit performance, several strategies have been utilized to reduce gate leakage at 27°C room temperature. A comparison of

CMOS 4:2 compressor circuit parameters such as transistor sizes, cell ratio, low power, output delay etc. and comparison results in summary for CMOS 4:2 Compressor and Proposed Novel CMOS 4:2 Compressor with DG FINFET Technique is shown below in Table 1.

Table 1 Summary of simulated results

Performance Parameter	**Conventional CMOS 4:2 Compressor**	**Proposed CMOS 4:2 Compressor**	**Proposed CMOS 4:2 Compressor Using DG-FinFET**
Technology Used	90 nm	90 nm	90 nm
Supply Voltage	0.7 V	0.7 V	0.7 V
Transistor Size	W = 120 nm, L = 100 nm	W = 120 nm, L = 100 nm	W = 120 nm, L = 100 nm
Cell Ratio	W/L = 1.2	W/L = 1.2	W/L = 1.2
Power Consumption	20.4 nW	18.4 nW	11.2 nW
Output Delay	80.8 ns	66.9 ns	40.3 ns
Power-Delay Product	1648.32 aJ	1230.96 aJ	451.36 aJ
Transistor Count	72	36	36
Area Used	Large	Small	Small

6. Conclusion

A compressor design based on the DG FinFET technology has been presented. According to the simulation findings, the DG FINFET technology may be employed to reduce the power dissipation in CMOS 4:2 compressor designs at a supply voltage of 0.7 V when compared to conventional CMOS 4:2 compressors. In comparison to the CMOS 4:2 compressor, the DG FINFET CMOS 4:2 compressor has a small area, and we were able to obtain the lowest power dissipation. By using the CADENCE VIRTUOSO Tool, simulation results are evaluated. Based on supply voltage Vdd=0.7 V, threshold voltage (0.35 V), and an input control voltage (0.7 V), the DG FINFET approaches have been described in this study. The use of DG FinFET methods provides higher performance from the 4:2 compressor than with the conventional CMOS 4:2 compressor.

Compliance with ethical standards

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Disclosure of conflict of interest

The authors declare no competing interests.

Statement of ethical approval

This is a simulation-based theoretical study that does not require ethical approval.

Author contributions

Pallavi Singh: Original draft writing, methodology, simulation and analysis.

Data availability

The dataset generated during analysis is available in the present article.

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