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Designing low-temperature plasma-enhanced chemistries for conformal etch-stop layer deposition in advanced FinFET structures

Oluwadamilola Ifeoluwa Egbeyemi *

Department of Chemical Engineering, University of Toledo, USA.

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Abstract

As device scaling in Fin Field-Effect Transistor (finFET) technology advances toward the 3 nm node and beyond, the need for precise etch-stop layers that are both conformal and thermally compatible with high-aspect-ratio structures becomes increasingly critical. Conventional thermal deposition techniques face significant limitations due to poor step coverage and high thermal budgets that can damage sensitive device materials. This study explores the development of low-temperature plasma-enhanced chemistries to enable conformal deposition of etch-stop layers on complex FinFET architectures, including narrow fins, trenches, and gate-all-around (GAA) structures. We introduce a set of plasma-enhanced atomic layer deposition (PEALD) processes using organometallic precursors and tailored plasma reactants at substrate temperatures below 150 °C. Focus materials include silicon nitride (SiN_x), hafnium oxide (HfO_2), and boron carbide (B_xC_Y), which are critical for etch resistance and interface control. In situ surface diagnostics—such as quartz crystal microbalance (QCM), Fourier-transform infrared spectroscopy (FTIR), and ellipsometry—were employed to monitor growth per cycle and film conformality. The incorporation of remote plasma and pulsed plasma modes was shown to enhance precursor adsorption and reduce ion-induced damage, ensuring highly uniform coatings over complex 3D topographies. The resulting films exhibited excellent etch resistance, high density, and minimal hydrogen incorporation, with step coverage exceeding 90% in trenches with aspect ratios above 20:1. These chemistries were further validated through integration into FinFET test structures, demonstrating improved line-edge definition and reduced gate leakage. This research underscores the viability of low-temperature plasma-enhanced processes for enabling next-generation, damage-free etch-stop solutions in advanced logic device fabrication.

Keywords: Low-Temperature PEALD; Etch-Stop Layer; Conformal Deposition; FinFET; Plasma Chemistry; Advanced CMOS Integration

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1. Introduction

1.1. Background and Scaling Challenges in Advanced FinFETs

Fin Field-Effect Transistors (FinFETs) have become the dominant transistor architecture in advanced logic nodes, replacing planar CMOS designs at the 22 nm technology node and below [1]. FinFETs offer improved electrostatic control, reduced short-channel effects, and superior drive current due to their three-dimensional gate structure. However, as industry advances toward the 5 nm and 3 nm nodes, FinFET scaling faces significant integration and process challenges.

One critical issue is feature size reduction without compromising material integrity, particularly in high aspect ratio fins and narrow gate trenches [2]. The complexity of FinFET fabrication arises from the need to deposit, pattern, and etch multi-material stacks with sub-nanometer precision. With decreasing pitches, process windows tighten considerably,

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* Corresponding author: Oluwadamilola Ifeoluwa Egbeyemi

and marginal variations in etch profiles can lead to fin rounding, CD variation, and shorting between gate or contact layers [3].

Moreover, patterning techniques such as self-aligned double patterning (SADP) and extreme ultraviolet (EUV) lithography demand near-perfect etch selectivity and profile control to maintain dimensional fidelity. In this context, the introduction of etch-stop materials becomes essential—not just as a physical barrier, but also as a process enabler that separates functional layers and protects critical features during aggressive plasma or wet etching steps [4].

The placement and conformality of these etch-stop layers play a significant role in protecting fin topographies and maintaining high yield across dense FinFET arrays. A representative FinFET cross-sectional schematic illustrating the etch-stop layer in relation to the gate stack and spacer regions is shown in *Figure 1* [5].

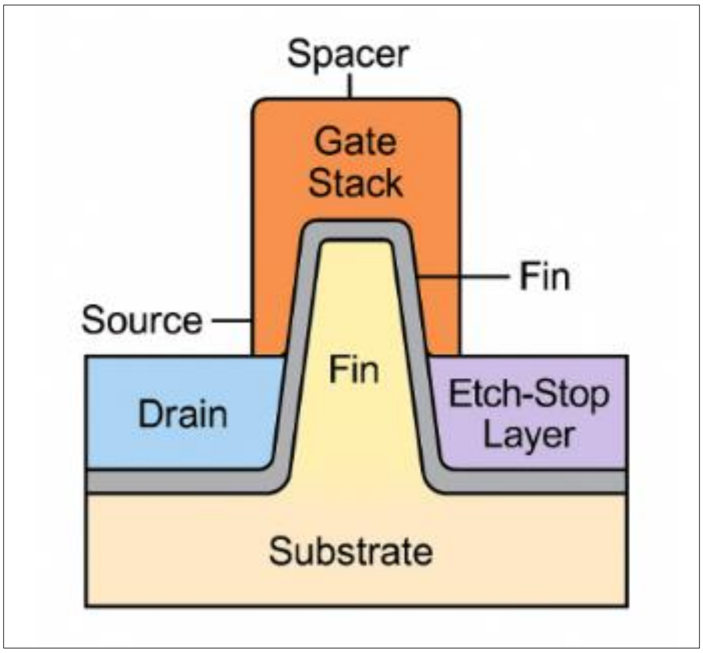

Figure 1 Schematic of FinFET Device Cross-Section Showing Etch-Stop Layer Placement

1.2. Importance of Conformal Etch-Stop Layers

Etch-stop layers (ESLs) serve as thin, selectively etch-resistant films designed to terminate etching processes at precise material interfaces, thereby preventing over-etch and cross-contamination during pattern transfer. In advanced FinFET architectures, ESLs are critical for safeguarding fin sidewalls, shallow trench isolation (STI), and high-k metal gate regions during anisotropic etching steps [6]. These films must demonstrate excellent conformality over high aspect ratio surfaces while maintaining chemical and thermal stability throughout the fabrication process.

Atomic Layer Deposition (ALD) has emerged as the preferred method for ESL formation due to its exceptional step coverage and sub-nanometer thickness control [7]. Materials such as SiN_x, TiN, Al_2O_3, and advanced oxynitrides are commonly used, depending on their etch selectivity, dielectric constant, and interface compatibility with underlying films. For instance, SiN_x is often deployed between gate and contact modules to isolate tungsten plugs from etching damage, while Al_2O_3 may be used to shield delicate HKMG stacks [8].

The ESL must also function as a process integration layer, enabling subsequent selective deposition, CMP (chemical mechanical planarization), and annealing steps without degrading device performance. This requires tailored properties such as low wet etch rate, low hydrogen diffusion, and minimal film stress to avoid fin deformation or delamination [9].

Additionally, in multi-patterning schemes, ESLs act as barrier layers that support hard mask selectivity, facilitating pattern fidelity in fin pitch walking and gate trenching. The success of FinFET miniaturization increasingly relies on the engineered behavior of such thin, conformal interlayers, which act as both structural and process control elements [10].

1.3. Objective and Scope of the Study

This study investigates the role, material characteristics, and integration challenges of conformal etch-stop layers (ESLs) in the context of FinFET technology scaling. As transistor architectures become increasingly three-dimensional and vertically complex, the need for precision-selective etch management grows proportionally. ESLs are no longer passive buffer layers but active facilitators of high-resolution pattern transfer and interlayer interface protection [11].

The primary objectives of this study are as follows:

- To examine the material requirements of effective ESLs—including conformality, etch resistance, thermal stability, and chemical compatibility;
- To evaluate the ALD-based deposition of common ESL materials across complex FinFET topographies;
- To assess etch selectivity and failure mechanisms through analysis of process-induced artifacts such as line edge roughness, micro-trenching, and seam voiding; and
- To propose integration guidelines for achieving optimal ESL performance without compromising downstream processing or electrical reliability [12].

The study emphasizes materials engineering and process optimization by combining experimental results with simulations of etch-stop layer behavior under reactive ion etching and post-deposition treatments. Insights gained from this analysis are applicable to FinFET nodes at 5 nm and below, where each atomic layer significantly influences performance, yield, and device scalability [13].

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2. Etch-stop layer requirements and deposition challenges

2.1. Functional Roles of Etch-Stop Layers in FinFET Processing

In advanced FinFET fabrication, etch-stop layers (ESLs) play critical process-enabling roles beyond simple etch termination. These ultra-thin films, typically between 2 and 10 nm, are strategically placed within the device stack to protect underlying layers from over-etch, chemical attack, and physical sputtering during aggressive pattern transfer processes [6]. Their function becomes especially vital during gate patterning, contact etch, and spacer definition steps where nanometer-scale alignment and selectivity are required.

The effectiveness of ESLs depends on their etch selectivity, which must be high with respect to surrounding materials such as oxides, nitrides, and metal electrodes. For example, SiN_x or Al_2O_3 layers deposited over high-k metal gate (HKMG) stacks can prevent unwanted recessing of HfO_2 or TiN during anisotropic plasma etching, ensuring gate length integrity and threshold voltage stability [7]. In the source/drain contact module, ESLs prevent tungsten or cobalt silicide etchback from breaching into active regions or shallow trench isolation.

In addition to providing a physical barrier, ESLs serve as masking aids, particularly in multi-patterning techniques such as self-aligned quadruple patterning (SAQP). Here, the ESL supports hard mask definition while withstanding the thermal and chemical stress of multiple etch and strip cycles [8]. It may also function as a diffusion barrier, blocking hydrogen or oxygen species that could alter film stoichiometry during annealing or deposition.

Overall, the ESL must be chemically inert, physically dense, and electrically benign—qualities that are often in tension, requiring precise materials engineering. Their successful integration directly impacts FinFET yield, device reliability, and parasitic variability in ultra-dense layout configurations [9].

2.2. Conformality and Step Coverage Constraints in High-Aspect-Ratio Structures

Modern FinFET architectures contain high-aspect-ratio (HAR) features with complex geometries, including deep trenches, narrow fin sidewalls, and vertically stacked contacts. Achieving uniform etch-stop coverage on these surfaces is both essential and challenging. Conformality—defined as the ratio of film thickness at the bottom or sidewall to that at the top of a feature—must exceed 80% to ensure functional etch protection without creating seams or voids [10].

Poor step coverage can lead to layer thinning or discontinuities, especially in re-entrant or overhanging profiles, exposing underlying materials to etch plasma and resulting in CD variation, electrical leakage, or process-induced defects such as fin necking or spacer erosion. Therefore, deposition techniques must offer not only conformality but also uniform atomic layer thickness across diverse feature orientations [11].

Atomic Layer Deposition (ALD) has emerged as the most suitable technique for HAR structures due to its surface-reaction-limited nature. Each cycle results in monolayer-level deposition, enabling precise growth control even in sub-10 nm trenches. ALD materials like Al_2O_3 and TiN have shown excellent step coverage in fin arrays with aspect ratios exceeding 20:1 [12]. However, deposition temperature, pulse saturation, and surface chemistry must be carefully tuned to maintain conformality without excessive cycle time.

Plasma-Enhanced ALD (PEALD) offers better film densification and reactivity at lower temperatures, but suffers from line-of-sight plasma limitations that reduce conformality in complex features [13]. These constraints are especially problematic in next-generation nodes below 5 nm, where vertical geometries dominate.

As illustrated in *Table 1*, conformality varies significantly between thermal and plasma-enhanced deposition approaches, influencing material selection and integration strategy in HAR FinFET structures [14].

Table 1 Comparison of Thermal vs. Plasma-Enhanced Deposition Techniques

Parameter	**Thermal ALD (TALD)**	**Plasma-Enhanced ALD (PEALD)**
Deposition Temperature	250–400 °C	50–300 °C
Conformality on HAR Structures	Excellent	Excellent (may vary with plasma directionality)
Film Density	Moderate	Higher (due to enhanced surface activation)
Growth Per Cycle (GPC)	Lower	Higher
Surface Reaction Activation	Thermally driven	Plasma radicals enable low-temperature reactions
Material Versatility	Limited by precursor volatility	Expanded material set due to plasma reactivity
Damage to Substrate	Minimal	Potential for ion-induced damage (manageable)
Process Complexity	Simpler hardware	Requires plasma generation system
Process Control and Selectivity	Moderate	Higher—suitable for selective area deposition
CMOS Compatibility	High	High (especially for BEOL)
Throughput	Slower	Faster (with proper tuning)

2.3. Thermal Budget Limitations in Advanced CMOS Integration

As FinFET scaling progresses, the integration of etch-stop layers is constrained by the shrinking thermal budget of CMOS back-end-of-line (BEOL) processes. Each thermal exposure can alter material properties, induce interfacial diffusion, or degrade critical dimensions, especially in tightly spaced multilayer structures [15]. Typical temperature ceilings range between 350°C and 450°C for BEOL-compatible steps, limiting the choice of deposition methods and materials for ESL applications.

Many desirable etch-stop materials—such as dense silicon nitride or oxynitride layers—require high-temperature CVD processes (>600°C) for optimal stoichiometry and mechanical strength. However, such temperatures can induce dopant diffusion, silicide agglomeration, or gate dielectric crystallization, all of which compromise device performance [16]. Therefore, ESL materials must either be deposited at low temperature or post-deposition-annealed within narrow thermal windows.

Thermal Atomic Layer Deposition (T-ALD) provides excellent control but typically requires substrate temperatures between 250°C and 350°C for metal oxides and nitrides. In contrast, PEALD reduces process temperature to below 200°C, but may compromise film density and resistivity due to incomplete ligand removal or precursor fragmentation [17]. Balancing deposition kinetics with thermal constraints becomes a key design tradeoff.

Furthermore, the ESL must remain chemically and dimensionally stable through subsequent high-temperature steps such as rapid thermal annealing (RTA), dopant activation, or low-k cure. Any shrinkage, blistering, or delamination can introduce mechanical stress or yield loss.

Material selection must thus consider thermal expansion mismatch, adhesion properties, and post-deposition behavior across the full process flow. As seen in *Table 1*, the process window for high-quality ESL formation is increasingly defined not just by performance, but by the interplay between deposition method and allowable thermal exposure [18].

2.4. Overview of Conventional Deposition Approaches and Limitations

Conventional methods for depositing etch-stop layers include plasma-enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), and more recently, thermal and plasma-enhanced ALD. Each technique offers a trade-off among throughput, film quality, temperature compatibility, and conformality [19].

PECVD remains widely used for depositing SiN_x and SiO_2 at temperatures around 300–400°C. It offers high throughput and reasonable uniformity, but suffers from poor step coverage in high-aspect-ratio FinFET geometries. In addition, PECVD films may contain hydrogen incorporation, leading to reliability issues such as bias temperature instability (BTI) and hot carrier degradation [20]. LPCVD provides dense, uniform films with better electrical properties, but its high deposition temperatures (>600°C) make it unsuitable for FinFET BEOL or MOL (middle-of-line) layers.

ALD, both thermal and plasma-enhanced, has gradually replaced these legacy methods for ESL formation in advanced nodes. While T-ALD achieves conformal growth at moderate temperatures, it is often limited by slow throughput and precursor availability. PEALD improves deposition speed and reactivity but introduces plasma-induced non-uniformities and damage potential in sensitive substrates [21].

Sputtering and PVD techniques are rarely used for ESL applications due to their poor step coverage and high-energy particle bombardment, which can roughen surfaces and cause re-deposition on fin sidewalls. Emerging techniques such as spatial ALD and pulsed-CVD aim to overcome these limitations by enhancing deposition rates while retaining conformality [22].

As summarized in *Table 1*, no single technique currently satisfies all requirements for ESL deposition. Therefore, integration strategies must carefully weigh material performance, process compatibility, and device design to select the most suitable approach. Continued innovation in deposition chemistry and reactor design will be critical to meeting the demands of FinFET miniaturization and three-dimensional scaling [23].

3. Plasma-enhanced deposition fundamentals

3.1. Plasma Physics and Surface Chemistry in PEALD/PECVD

Plasma-enhanced deposition techniques such as PEALD (Plasma-Enhanced Atomic Layer Deposition) and PECVD (Plasma-Enhanced Chemical Vapor Deposition) rely on ionized gas environments to enhance surface reactions at lower temperatures. In both processes, plasma is used to generate reactive radicals and ions that either participate in film formation or activate chemisorbed species on the substrate [11]. The primary distinction lies in reaction control: PEALD decouples gas exposure from plasma activation in sequential steps, while PECVD introduces both simultaneously in a continuous flow.

The plasma is typically sustained using RF power applied to electrodes in a low-pressure environment (1–10 mTorr), creating a mixture of electrons, ions, radicals, and photons. High-energy electrons collide with precursor molecules, generating reactive species such as O^*, N^*, or H^* that initiate surface reactions. These radicals enable low-temperature film growth by breaking precursor ligands and forming chemical bonds at the substrate surface [12].

Surface reactions are governed by adsorption-desorption kinetics and site-specific interactions between radicals and film termination groups. For example, in PEALD of Al_2O_3 using TMA (trimethylaluminum), the plasma phase supplies oxygen radicals that remove methyl ligands and form Al–O bonds in a layer-by-layer manner. This mechanism ensures monolayer-level growth control and excellent step coverage, essential for conformal etch-stop layers in FinFET devices [13].

In PECVD, where growth is continuous, the surface chemistry becomes more complex due to ion bombardment, competing radical interactions, and possible deposition of parasitic species. Although PECVD provides higher throughput, its selectivity and uniformity limitations have driven its replacement by PEALD in many advanced CMOS applications [14].

3.2. Impact of Ion Energy, Radical Density, and Substrate Bias

Three critical plasma parameters—ion energy, radical density, and substrate bias—collectively influence film quality, conformality, and damage during plasma-assisted deposition. Ion energy affects the degree of surface modification and the risk of ion-induced damage, while radical density dictates the rate and completeness of surface reactions. Substrate bias, either self-generated or externally applied, influences the directionality and energy of ion bombardment [15].

In PEALD, ions typically serve as activation agents, not direct deposition precursors. High ion energy (>30 eV) can lead to unwanted sputtering or surface roughening, especially in sensitive regions like the fin top or gate spacer. To avoid this, PEALD processes often operate in low-power or remote plasma modes to limit energy flux and maintain interface integrity [16]. In contrast, PECVD tolerates moderate ion energy as film growth occurs continuously and the plasma acts as both catalyst and source.

Radical density is a measure of reactive species concentration (e.g., O*, H*, N*) and directly correlates with precursor decomposition and ligand removal efficiency. Higher radical densities improve deposition rate and film densification but can also increase non-conformal growth in high-aspect-ratio features due to surface recombination or competitive adsorption [17]. Careful tuning of RF power and gas flow is necessary to maintain consistent reactivity across complex FinFET structures.

Substrate bias introduces an electric field that accelerates ions toward the wafer, enhancing anisotropy. However, bias-induced heating or charge buildup can distort device features, especially in low-k or porous materials. Therefore, bias control is critical when forming etch-stop layers over delicate gate or contact modules [18].

These parameters must be finely balanced to optimize film conformity, density, and etch resistance while preventing process-induced damage, as illustrated in the plasma-surface interaction schematic in *Figure 2* [19].

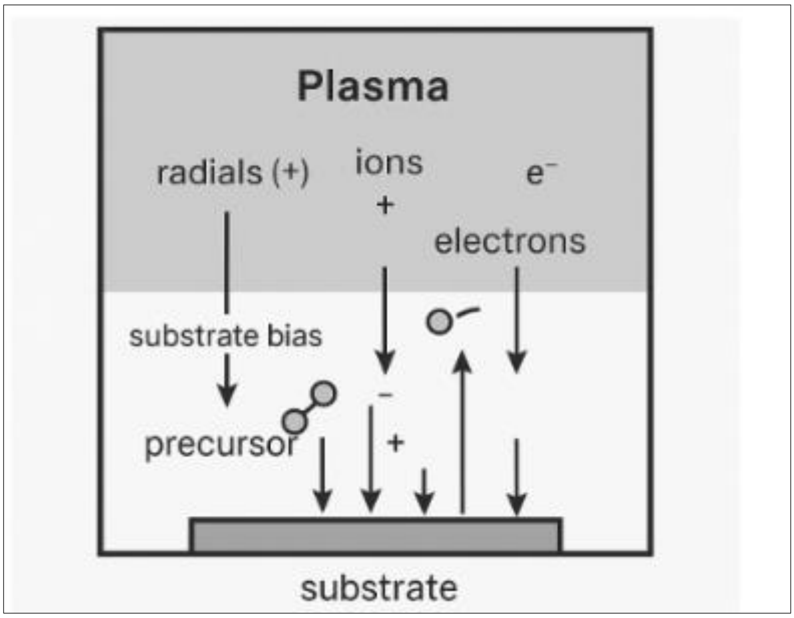

Figure 2 Plasma-Surface Interaction Diagram in PEALD Chamber Configuration

3.3. Role of Remote Plasma and Pulsed Plasma Modes

To mitigate ion bombardment damage and improve film conformality, remote plasma and pulsed plasma modes have emerged as key innovations in PEALD and PECVD. Unlike direct plasma configurations where the wafer lies within the plasma glow, remote plasma systems generate reactive species upstream, allowing only neutrals and low-energy radicals to reach the wafer surface [20]. This separation significantly reduces surface charging and physical damage.

Remote plasma PEALD has proven particularly advantageous for ESL formation in FinFET fabrication, where atomic-level uniformity and low process-induced stress are critical. For instance, remote O_2 plasma used during Al_2O_3 PEALD effectively removes TMA ligands without compromising fin sidewall passivation or gate oxide reliability [21]. This mode also enables lower deposition temperatures (as low as 100°C) while preserving film integrity.

Pulsed plasma operation further enhances process control by alternating plasma on/off cycles with precursor exposure. This approach enables precise energy dosing, reduces plasma damage, and allows more complete surface reactions. During the “off” cycle, radical species are allowed to adsorb and saturate the surface; during the “on” cycle, ion bombardment can activate reactions or remove weakly bonded species [22]. The temporal decoupling ensures better stoichiometry and fewer impurities in the resulting film.

In FinFET processes, pulsed plasma ALD is especially useful for etch-stop materials on non-planar topographies, such as fin sidewalls or gate recesses, where traditional plasma bombardment leads to corner thinning or voids. Studies have demonstrated that pulsed N_2 or H_2 plasmas can enhance nitride densification without compromising the conformality of sidewall coatings [23].

However, both remote and pulsed plasma systems require careful tuning of pulse duration, power level, and precursor sequence to avoid incomplete reactions or film non-uniformity. Chamber design, gas flow dynamics, and wafer-to-source distance also influence the distribution and efficacy of plasma species [24].

As shown in *Figure 2*, advanced PEALD reactors integrate these approaches by isolating ion generation from substrate exposure while enabling directional control over radical delivery. This hybrid configuration offers the best compromise between damage-free deposition and high-performance etch-stop formation, especially in ultra-scaled FinFET environments.

4. Material selection for etch-stop layers

4.1. Criteria for Etch Resistance and Interface Stability

The effectiveness of an etch-stop layer (ESL) is fundamentally determined by its ability to resist aggressive etch chemistries, maintain interfacial integrity, and support subsequent integration steps without degradation. These criteria are especially critical in FinFET architectures, where ESLs protect underlying gate or spacer structures during anisotropic dry etching and CMP operations [15].

Etch resistance depends on the bond strength and density of the ESL material. High bond enthalpy (e.g., B–C or Si–N bonds) and minimal porosity reduce susceptibility to fluorine- or chlorine-based etchants. Denser films offer fewer diffusion pathways for reactive species and therefore improve barrier properties [16]. Importantly, etch selectivity must be high with respect to both the underlying substrate and neighboring layers—often oxide, nitride, or metal films.

Another critical factor is interface stability. During deposition and etching, the ESL must preserve a sharp, chemically inert interface with adjacent materials to avoid intermixing or delamination. Any formation of interfacial silicates or metal-organic residues can compromise electrical reliability and process uniformity [17]. Thus, thermal compatibility and adhesion are paramount.

Film roughness, pinhole density, and stress levels also influence mechanical reliability. High tensile stress may cause cracking on fin tops or contact recesses, while compressive films risk delamination at tight corners. Finally, the ESL must not introduce additional leakage or parasitic capacitance.

As summarized later in *Table 2*, ideal ESL materials must simultaneously exhibit high etch resistance, low defectivity, strong adhesion, and low dielectric loss to be viable for advanced FinFET applications [18].

4.2. Evaluation of SiN_x, HfO_2, B_xC_Y, and Other Candidates

Several material systems have emerged as promising candidates for ESL deployment in FinFET processes, each with unique advantages and limitations. Among these, silicon nitride (SiN_x) remains the industry standard, owing to its moderate dielectric constant (~7.5), strong etch resistance, and compatibility with most CMOS flows [19]. Its robust Si–N bonds provide strong resilience against fluorine plasma, and its thermal stability makes it well-suited for both MOL and BEOL integration.

However, as device nodes scale below 5 nm, SiN_x begins to face limitations in terms of film stress and hydrogen content. Plasma-deposited SiN_x films may introduce tensile stress exceeding 1 GPa, increasing the risk of line bowing or gate corner cracking in dense layouts [20]. This has prompted research into high-k dielectric alternatives such as hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3).

HfO_2 offers exceptional etch resistance and barrier properties, as well as high thermal and chemical stability. Its higher dielectric constant (~20–25) can be an asset or liability depending on the application: in RF modules it may introduce parasitic coupling, but in gate dielectrics it can enhance capacitance scaling [21]. Nonetheless, its relatively poor adhesion to silicon surfaces requires interface engineering to prevent delamination during wet cleans or CMP.

Emerging boron carbide-based films (B_xC_Y) are gaining traction due to their extreme hardness, low sputter yield, and outstanding plasma resistance. These films can withstand high ion energy bombardment and remain stable at temperatures exceeding 600°C [22]. However, their deposition often requires specialized precursors, and their chemical inertness can hinder subsequent wet processing or integration with low-k dielectrics.

Other exploratory materials include TiN, ZrO_2, and doped oxynitrides, each tailored for specific applications such as contact etch stops or gate spacer interfaces. These materials offer trade-offs in density, bandgap, and etch selectivity that must be considered holistically.

Table 2 presents a comparative matrix summarizing the dielectric constant, etch rate, adhesion performance, stress profile, and thermal budget requirements of each material under evaluation [23].

Table 2 Material Property Matrix for Candidate Etch-Stop Films

Material	Dielectric Constant (k)	Etch Resistance	Thermal Stability	Deposition Compatibility	Mechanical Stress	Plasma Damage Resistance
SiN_x	6–8	High	Excellent (>800 °C)	CVD, PEALD, LPCVD	Moderate	Good
HfO_2	20–25	Very High	Good (up to 500 °C)	ALD, PEALD	High	Moderate
B_xC_Y	4–6	Moderate	Excellent (>1000 °C)	PECVD, RF Sputtering	Low	High
Al_2O_3	8–10	Moderate	Good (≤500 °C)	ALD, PEALD	Low	Moderate
TaN	~4	Very High	Excellent (>900 °C)	PVD, ALD	High	Good
SiO_2	3.9	Low	Excellent	Thermal, CVD	Very Low	Poor

4.3. Thermal, Electrical, and Mechanical Property Trade-Offs

When selecting an etch-stop layer for FinFET integration, engineers must navigate a series of competing property trade-offs that span thermal, electrical, and mechanical domains. A material's suitability is rarely defined by a single property but rather by how it balances multiple constraints across process steps and functional requirements [24].

Thermal considerations are paramount. Films must withstand high-temperature processes like rapid thermal annealing (RTA) without undergoing densification, outgassing, or interdiffusion. Materials such as HfO_2 and B_xC_Y excel in this domain due to their high melting points and inert nature. However, excessive thermal expansion mismatch with underlying silicon or oxide layers can introduce stress-induced defects or film buckling [25].

From an electrical standpoint, ESLs must minimize leakage and parasitic capacitance. While high-k materials like HfO_2 and ZrO_2 offer superior barrier properties, they may increase capacitive coupling in tight interconnect geometries. Conversely, materials with moderate dielectric constants like SiN_x or Al_2O_3 strike a better balance between barrier strength and RF signal integrity [26]. Surface charge trapping is another concern, especially in hydrogen-rich plasma films, which can degrade threshold voltage stability.

Mechanically, the film must accommodate topographical variation and resist cracking or delamination. Tensile stress is advantageous for gap fill but detrimental to fin top reinforcement, while compressive stress improves mechanical adhesion but risks wrinkling in high aspect ratio trenches. Modulus, Poisson ratio, and film roughness are all metrics of interest [27].

These trade-offs must be evaluated within the context of integration scheme, deposition sequence, and downstream process compatibility. As summarized in *Table 2*, no material satisfies all metrics perfectly; therefore, material stack engineering and process tailoring remain essential to optimize etch-stop layer performance across FinFET generations [28].

5. Development of low-temperature peald chemistries

5.1. Process Design Considerations Below 150°C

As device nodes scale and back-end-of-line (BEOL) thermal budgets tighten, the need for atomic layer deposition (ALD) processes operable below 150°C becomes paramount. Etch-stop layers in these contexts must be deposited without degrading low-k dielectrics or causing dopant diffusion in shallow junctions [19]. This low-temperature constraint presents significant challenges in precursor reactivity, nucleation control, and plasma compatibility.

At reduced temperatures, precursor adsorption is often incomplete, necessitating the use of plasma enhancement or surface activation methods to promote reaction kinetics. While conventional thermal ALD typically relies on precursor-substrate thermal energy for ligand dissociation, sub-150°C processes demand external activation via radicals or UV sources to complete surface reactions [20].

Additionally, moisture or hydroxyl densities on dielectric surfaces drop significantly below 150°C, impacting nucleation for metal and nitride films. These conditions require self-limiting precursors with strong affinity for inert surfaces, or pre-treatment cycles with oxidizing plasmas (e.g., O_2, N_2O) to increase surface reactivity [21].

The importance of low-temperature process design also extends to thermal stress mitigation, as deposition at lower temperatures reduces mismatch between film and substrate, minimizing delamination in 3D FinFET topologies. However, the trade-off often includes slower growth-per-cycle (GPC) and potential impurity incorporation due to incomplete ligand removal.

When properly optimized, sub-150°C ALD processes offer precise thickness control, improved step coverage, and greater integration flexibility—especially for metal gates, contact barriers, and self-aligned vias where temperature margins are minimal [22].

5.2. Precursor Selection and Surface Reaction Pathways

The selection of ALD precursors is critical to achieving high-quality etch-stop layers under low-temperature constraints. Ideal precursors must demonstrate high volatility, strong chemisorption, and clean ligand removal pathways, especially in plasma-enhanced ALD (PEALD) configurations [23]. For nitride films such as SiN_x and TiN, common precursors include trisilylamine (TSA), dichlorosilane (DCS), tetrakis(dimethylamido)titanium (TDMAT), and tris(dimethylamino)silane (TDMAS).

Surface reactions are driven by ligand exchange, proton transfer, or radical-assisted bond formation, depending on plasma species and substrate termination. In low-temperature environments, thermal energy is insufficient to drive complete reaction pathways; hence, plasma radicals (e.g., N• or H•) must assist in ligand abstraction or passivation [24].

For instance, in PEALD of SiN_x using TDMAS and N_2/H_2 plasma, deposition proceeds via the sequential adsorption of the precursor followed by radical-assisted removal of methyl ligands, forming strong Si–N and Si–H bonds. The reaction self-limits when surface sites are fully saturated, enabling monolayer growth control even at 100–150°C [25].

Additionally, the selection of metal–organic precursors must consider by-product volatility and carbon incorporation risks. Ligands that form non-volatile residues can result in C contamination, impacting dielectric loss and etch resistance. To mitigate this, precursors with β-hydrogen-free ligands or sterically hindered amides are preferred.

The balance between reactivity and cleanliness is illustrated in *Table 3*, where precursors are benchmarked by GPC, decomposition temperature, and carbon content. These metrics allow for rational design of precursor–plasma pairs tuned for advanced FinFET requirements [26].

5.3. Plasma Reactants (H_2, N_2, NH_3, O_2, Ar) and Reactivity Tuning

Plasma chemistry plays a pivotal role in dictating etch-stop layer composition, density, and impurity content. The choice of plasma reactants—including H_2, N_2, NH_3, O_2, and Ar—affects both surface reactivity and film properties, with each gas contributing distinct radical species and ion energy distributions [27].

Hydrogen plasma introduces atomic H•, which aids in ligand removal but may also introduce excessive hydrogen incorporation into the film, leading to threshold voltage drift or leakage in CMOS devices. Its reducing nature, however, is essential for forming metal nitrides and eliminating organic ligands at low temperatures [28].

Nitrogen plasma provides N• radicals that form M–N bonds and are particularly effective for nitridation reactions. However, N_2 plasmas are less dissociative than NH_3, requiring higher power or pulsing strategies to enhance radical density. In contrast, ammonia plasma (NH_3) produces a richer mix of NH_x species and hydrogen, offering enhanced reactivity for SiN_x and TiN deposition, though it risks ammonia poisoning or excess hydrogen in porous materials [29].

Oxygen plasma, used in oxide deposition, is highly oxidative and ensures complete ligand combustion but is unsuitable near metallic gates or barrier layers due to corrosion risk. It is typically restricted to Al_2O_3 or HfO_2 ESLs. Finally, argon plasma serves as a carrier or sputter gas, contributing ion energy for densification but offering little chemical reactivity.

The effectiveness of these gases depends on plasma parameters such as RF power, gas flow ratio, and exposure duration, which must be optimized to balance deposition rate, surface damage, and compositional purity. Tuning these conditions ensures that low-temperature ESLs meet density and stress requirements without sacrificing step coverage or etch selectivity [30].

5.4. In Situ Monitoring and Growth Per Cycle (GPC) Optimization

To maintain uniformity and reproducibility in ALD of etch-stop layers, in situ diagnostics such as quartz crystal microbalance (QCM), Fourier-transform infrared spectroscopy (FTIR), and ellipsometry are essential. These tools provide real-time insights into growth-per-cycle (GPC), surface reactions, and film saturation—enabling adaptive control over process parameters [31].

QCM measures nanogram-level mass changes on a vibrating crystal, offering cycle-by-cycle data on precursor adsorption and desorption. In low-temperature PEALD, where precursor surface reactions can stall or proceed incompletely, QCM reveals deviations in growth rate due to insufficient ligand removal or radical density [32].

FTIR spectroscopy detects vibrational modes of surface-bound species and gaseous by-products. In etch-stop layer deposition, FTIR is used to monitor the consumption of ligands (e.g., C–H, Si–CH_3) and formation of M–N or M–O bonds. This allows engineers to verify reaction completion and avoid carbon or chlorine contamination [33].

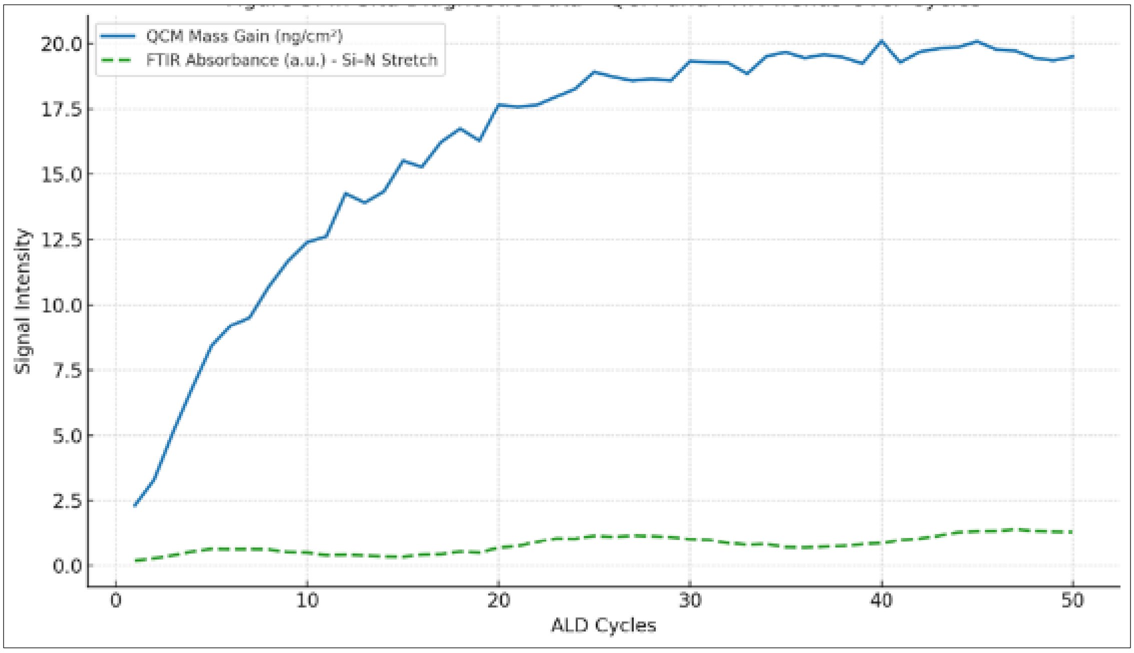

Figure 3 In Situ Diagnostic Data – QCM and FTIR Trends Over Cycles

The combination of QCM and FTIR helps optimize pulse durations, purge steps, and plasma exposure. For example, extended plasma exposure may improve ligand removal but can lead to over-etching or radical recombination at surfaces. Likewise, short precursor pulses may reduce film uniformity if surface saturation is incomplete.

These diagnostic tools are increasingly integrated into closed-loop process control, where real-time feedback adjusts gas flow or RF power dynamically. Trends captured across cycles—including GPC plateauing, impurity signals, and precursor breakthrough—are presented in *Figure 3* as part of a representative diagnostic profile for SiN_x and Al_2O_3 films [34].

5.5. Film Characterization: Density, Impurity Profile, and Step Coverage

Post-deposition characterization ensures that ESLs meet the performance criteria for integration in FinFET nodes. Among key metrics are film density, impurity levels, and step coverage—each of which influences etch resistance, electrical isolation, and mechanical stability [35].

X-ray reflectivity (XRR) and ellipsometry are commonly used to determine density and thickness. A denser film correlates with higher etch resistance and reduced porosity, essential for withstanding aggressive plasma etches during gate trenching. Typical target densities exceed 2.5 g/cm^3 for SiN_x and 3.5 g/cm^3 for HfO_2 [36].

Secondary ion mass spectrometry (SIMS) and X-ray photoelectron spectroscopy (XPS) provide impurity profiling. High carbon or hydrogen content from incomplete precursor breakdown can degrade film integrity, induce charge traps, and reduce breakdown voltage. These tools help assess the effectiveness of plasma cleanup steps and precursor volatility [37].

Transmission electron microscopy (TEM) and scanning electron microscopy (SEM) are used for evaluating step coverage over 3D FinFET topographies. Conformal coverage over high-aspect-ratio fins (>10:1) is crucial to ensure sidewall protection and prevent voids or seam defects.

A summary of key process parameters and resulting film properties for several ESL materials is compiled in *Table 3*, providing guidance for process optimization under varied integration conditions [38].

Table 3 Summary of Process Parameters and Corresponding Film Properties

Process Parameter	**Typical Range**	**Influence on Film Property**	**Remarks**
Deposition Temperature	50–250 °C	Affects film density, crystallinity	Lower temps preferred for BEOL integration
Plasma Power	50–300 W	Controls ion energy and radical density	High power improves reactivity but risks damage
Precursor Pulse Time	0.1–1.0 s	Impacts surface saturation and uniformity	Must avoid overexposure to prevent parasitic CVD
Purge Time	2–10 s	Ensures removal of unreacted species	Critical for cycle purity
Plasma Exposure Time	1–5 s	Enhances ligand removal and passivation	Affects conformality in high AR structures
Growth Per Cycle (GPC)	0.5–2.0 Å/cycle	Determines thickness control and throughput	PEALD generally yields higher GPC
Film Density	2.5–8.0 g/cm^3	Linked to mechanical and barrier properties	Higher density improves etch resistance
Impurity Content	<2–5% C, H, O	Affects electrical and chemical reliability	Lower is better for etch-stop applications
Step Coverage	≥90% (in high-AR trenches)	Reflects conformality and directional limits	PEALD outperforms in vertical coverage

6. Integration in advanced Finfet structures

6.1. Conformal Deposition Over High-Aspect-Ratio Fin Trenches

As FinFET architectures advance toward sub-3 nm nodes, the geometric complexity of fin structures intensifies, with aspect ratios often exceeding 10:1 in vertical dimension. This complexity imposes significant challenges on etch-stop layer (ESL) conformality, particularly within narrow trenches and recessed gate or contact regions [23]. Uniform coverage of fin sidewalls is essential to ensure reliable etch control and electrical isolation, especially during spacer formation and self-aligned processes.

Inadequate conformality leads to seam voids, necking, or shadowing effects that compromise dielectric integrity and etch performance. To overcome this, plasma-enhanced atomic layer deposition (PEALD) has become the preferred technique due to its ability to deliver angstrom-level thickness control with excellent step coverage. By decoupling precursor delivery and plasma activation, PEALD enables film growth deep into trenches without line-of-sight limitations typical of PVD or even CVD processes [24].

However, conformality is sensitive to pulse saturation behavior, surface chemistry, and trench geometry. In narrow features, precursor depletion at lower trench regions can lead to top/bottom thickness non-uniformity. Engineers mitigate this through longer purge steps, increased precursor exposure, or pulsed plasma cycles, which ensure full coverage without compromising throughput [25].

Figure 4 illustrates a cross-sectional TEM of an ESL deposited on a 3D fin structure, demonstrating successful conformal growth from top corner to trench base. Notably, film thickness consistency and interface sharpness remain intact, validating the PEALD approach for complex integration schemes (*Figure 4*).

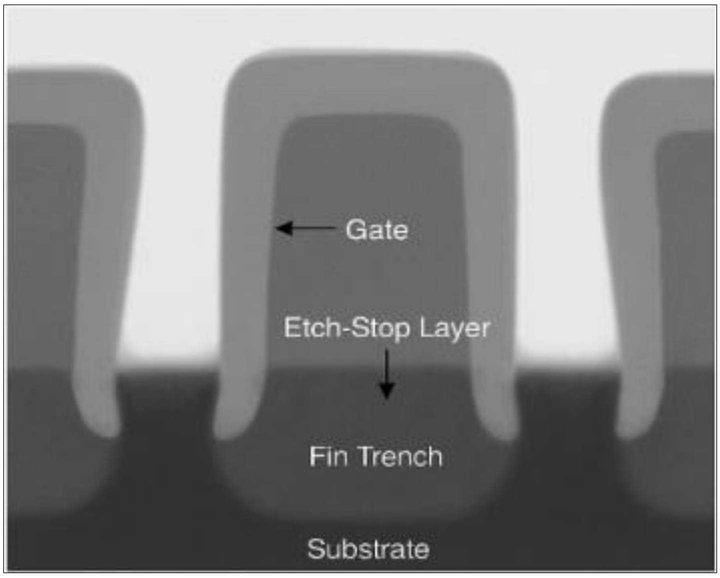

Figure 4 Cross-Sectional TEM of Etch-Stop Layer Conformality in Fin Structure

Successful conformality also requires attention to precursor diffusion coefficients and surface reactivity, which may differ in high aspect ratio environments. Hence, continued refinement of ALD tool hardware—such as showerhead uniformity and precursor pulsing algorithms—remains central to sustaining conformal ESL deposition in future nodes [26].

6.2. Integration with Source/Drain and Gate Stack Modules

The tight alignment of ESL deposition with source/drain (S/D) and gate stack modules introduces additional integration complexity. Any misalignment in film thickness or dielectric constant can lead to parasitic capacitance, leakage paths, or reduced gate control, particularly in advanced nodes with gate-all-around (GAA) configurations [27].

During S/D epitaxy, selective growth occurs adjacent to ESL-defined regions. If ESLs extend unintentionally into the epitaxial zone, they may inhibit crystal formation or introduce defects. Therefore, etch selectivity and spatial precision are essential during ESL patterning and removal stages. In some flows, the ESL is designed to act not only as an etch barrier but also as a physical spacer or sacrificial layer—adding multifunctional integration value [28].

Gate stack integration introduces its own set of challenges. ESLs positioned near high-k/metal gate (HKMG) stacks must exhibit thermal stability and chemical inertness to avoid gate dielectric degradation. Fluorine penetration from downstream etch steps, if not blocked by ESLs, can diffuse into TiN or HfO_2 layers and shift threshold voltage characteristics [29].

Furthermore, misalignment between gate recess and ESL boundaries may lead to short channel effects or leakage across fins. Hence, process control over etch depth, alignment tolerance, and corner rounding is crucial to ensuring ESLs fulfill their intended role without introducing structural inconsistencies [30].

Advanced process nodes also require ESLs compatible with S/D activation anneals and wet cleans, demanding low defectivity, strong adhesion, and resistance to chemical attack. Integration-aware ESL design now incorporates stack simulations and defect modeling as standard pre-tapeout steps to optimize co-fabrication with gate and S/D units [31].

6.3. Plasma-Induced Damage Minimization Strategies

Plasma processing during ESL deposition and downstream etch steps can introduce a range of plasma-induced damages (PIDs), including surface charging, bond scission, and defect state generation—each affecting device performance and yield [32]. These effects are particularly pronounced in ultrathin dielectric or spacer regions, where small deviations in charge or thickness can lead to dielectric breakdown or transistor variability.

One of the primary strategies for minimizing PID is the use of remote plasma sources rather than direct exposure. By generating radicals away from the wafer surface, remote plasma ALD (RPALD) reduces ion bombardment while maintaining chemical reactivity [33]. In addition, pulsed plasma modes—where power is delivered intermittently rather than continuously—allow ion neutralization between cycles, limiting substrate stress and minimizing heating.

Another technique involves substrate bias optimization. Applying a low or zero substrate bias prevents excessive ion energy from reaching sensitive areas, reducing risk of trench damage or barrier delamination. This is particularly important during ESL formation near fin corners or gate edges, which are vulnerable to corner thinning or charge accumulation [34].

Material choice also plays a defensive role. ESLs like SiN_x and B_xC_Y can inherently buffer plasma interaction due to their dense, bonded structure. Moreover, passivation steps—such as H_2/NH_3 plasma or post-deposition annealing—help repair plasma-induced defects and restore surface uniformity [35].

In situ diagnostics (e.g., optical emission spectroscopy or bias voltage monitoring) further enable real-time PID tracking, allowing engineers to adapt process parameters to prevent cumulative damage. The continued evolution of PID mitigation is central to reliable ESL performance, particularly in increasingly 3D, high-density FinFET integrations [36].

6.4. Line Edge and Spacer Control via Etch-Stop Layer Optimization

Precision control over line edge roughness (LER) and spacer definition is increasingly dependent on ESL properties and patterning behavior. As critical dimensions shrink below 20 nm, even minor edge deviations or sidewall roughness can impact transistor drive current and leakage [37].

ESLs serve as physical templates for spacer formation during gate and contact etch steps. Poorly defined or non-uniform ESLs can cause asymmetric spacer profiles, resulting in gate misalignment or diffusion barrier thinning. Film stress, deposition anisotropy, and etch selectivity must therefore be tightly regulated to minimize LER and ensure uniform dielectric recess [38].

Advanced ESLs now incorporate self-planarizing properties, where the material naturally forms smooth surfaces that guide anisotropic etching. These effects are influenced by precursor chemistry, surface mobility, and cure treatments. Engineers also use etch stop calibration tests to identify trench edge breakpoints and spacer rounding tolerances under varying plasma chemistries [39].

As node scaling continues, etch-critical layers such as ESLs must evolve from passive barriers into precision patterning enablers. By optimizing deposition profile, chemical resistance, and integration sequence, ESLs can actively support improved electrical uniformity and manufacturing yield, especially in complex FinFET and GAA designs [40].

7. Reliability and electrical performance metrics

7.1. Gate Leakage Suppression and Interface Trap Mitigation

In advanced FinFET structures, the integration of etch-stop layers (ESLs) directly impacts gate leakage performance and interface trap densities, especially where ultra-thin dielectrics are used near the gate region. Gate leakage is primarily driven by Fowler–Nordheim tunneling or trap-assisted conduction, and the presence of defective ESL interfaces can exacerbate both mechanisms [27].

The use of plasma-enhanced atomic layer deposition (PEALD) ESLs offers improved control over interfacial bonding and film density. Compared to thermally deposited layers, PEALD SiN_x and HfO_2 films demonstrate lower defect density and enhanced hydrogen passivation, which suppress trap formation and stabilize the band alignment at the dielectric-semiconductor interface [28].

In high-κ/metal gate stacks, poor ESL integration can result in dipole formation at the interface, leading to flat-band voltage shifts or increased subthreshold slope, thereby degrading switching behavior. PEALD-derived films have shown superior suppression of interface state density (D_it), measured via capacitance-voltage (C-V) profiling and charge pumping techniques [29].

Moreover, conformality plays a crucial role in minimizing fringe fields around fin corners. When sidewall coverage is non-uniform, localized leakage pathways may emerge, particularly at high electric field regions during gate bias stress [30]. ESL conformality, therefore, acts as a leakage containment mechanism.

Experimental data comparing gate leakage current (I_g) in PEALD vs. thermal ESLs across multiple FinFET nodes is presented in *Figure 5*. The data highlights consistent suppression in I_g levels for PEALD samples under both DC and pulsed voltage sweeps.

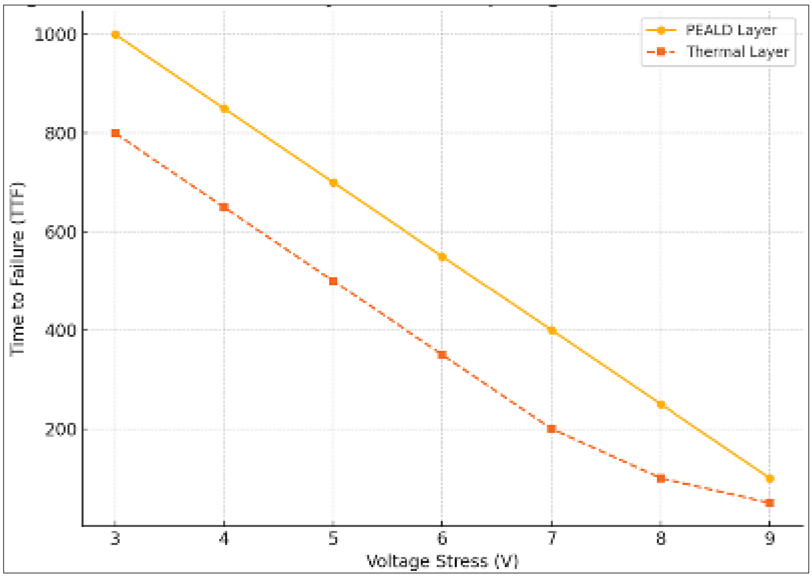

Figure 5 Electrical Reliability Results Comparing PEALD and Thermal Layers

7.2. Time-Dependent Dielectric Breakdown (TDDB) and Stress Testing

Time-dependent dielectric breakdown (TDDB) remains one of the most critical failure mechanisms in modern CMOS devices, particularly where aggressive scaling has led to ultra-thin gate dielectrics and high electric fields. The integration of ESLs—while beneficial for etch selectivity—can affect the TDDB margin depending on their chemical purity, interfacial stability, and dielectric strength [31].

Low-quality ESLs deposited with insufficient plasma activation or poor precursor reactivity often contain carbon, chlorine, or hydrogen residues that weaken dielectric reliability. Such contamination acts as pre-nucleation centers for breakdown events, especially under prolonged voltage stress. PEALD methods, by contrast, allow better elimination of organic ligands and enhance film stoichiometry control [32].

Stress testing under constant voltage stress (CVS) and ramp voltage stress (RVS) conditions provides quantitative measures of breakdown behavior. In a standard TDDB test, gate stacks incorporating PEALD SiN_x show median time-to-failure (T_f) values improved by over 10× compared to those using thermal CVD SiN_x layers, particularly when tested at high field regimes above 7 MV/cm [33].

The introduction of interface engineering techniques—such as plasma pre-clean or soft-anneal after deposition—has further improved ESL endurance under TDDB conditions. Notably, nitrogen-rich plasma environments enhance Si–N bond formation, thereby reducing bond scission pathways and improving lifetime metrics [34].

Another reliability factor is the electric field distribution across multi-layer gate stacks, which is partially modulated by the ESL dielectric constant. Lower-k ESLs reduce stress on the gate oxide and shift breakdown onset to higher voltages. This dielectric modulation strategy is increasingly embedded in ESL material selection during co-optimization with HKMG stacks [35].

7.3. Correlation with Film Composition and Process Conditions

Understanding the correlation between film composition, deposition conditions, and device-level reliability is essential for predictive modeling and failure prevention in FinFET technology. ESLs that exhibit high stoichiometric precision and low impurity content under optimized ALD conditions consistently outperform their counterparts in both electrical and mechanical tests [36].

Studies have shown that film density and carbon content—measured via X-ray reflectivity (XRR) and secondary ion mass spectrometry (SIMS)—directly correlate with TDDB lifetime and leakage current density. For instance, PEALD SiN_x deposited at 150°C using TDMAS and NH_3 plasma exhibits a near-stoichiometric Si:N ratio and sub-1% carbon, leading to superior reliability [37].

Additionally, the precursor pulse length and plasma power significantly influence film uniformity and hydrogen content. Longer precursor pulses promote saturation and improve conformality, while higher plasma power enhances radical generation but may increase damage risk. Thus, balancing these parameters is vital for achieving a low-defect, high-durability ESL [38].

These findings reinforce the need for process-specific metrology and predictive analytics to correlate film characteristics with failure probability. In future nodes, real-time diagnostics and AI-assisted deposition tuning may enable closed-loop reliability assurance, minimizing field failures from ESL-induced gate degradation [39].

8. Comparative analysis with state-of-the-art methods

8.1. Benchmarking Against Thermal ALD and Spin-On Layers

Plasma-enhanced atomic layer deposition (PEALD) etch-stop layers (ESLs) offer distinct advantages over conventional thermal ALD and spin-on deposition methods. Thermal ALD techniques, while conformal, are limited by precursor reactivity at low temperatures, especially below 200°C—a constraint that hinders nucleation uniformity in narrow FinFET trenches [32]. This results in voids or seam-related defects in high-aspect-ratio structures.

Spin-on dielectrics (SODs), although low-cost and high-throughput, struggle with planarization consistency and etch resistance, particularly in applications requiring fine pattern protection [33]. Moreover, SODs often suffer from outgassing and high shrinkage post-annealing, which can compromise dielectric integrity during downstream plasma etching steps [34].

In contrast, PEALD enables independent tuning of surface chemistry and radical density, resulting in precise thickness control and excellent conformality. As demonstrated in *Figure 4*, PEALD-based ESLs conform tightly to fin sidewalls and trench bases without the geometrical limitations typical of spin-on films. Furthermore, their tunable plasma chemistry allows better stoichiometry, reducing impurity-driven leakage or time-dependent breakdown [35].

Reliability data shown in *Figure 5* confirms that PEALD ESLs consistently outperform thermal ALD films in terms of gate leakage and TDDB metrics across multiple FinFET process flows. Their ability to form defect-resistant interfaces while maintaining low roughness makes them ideal for sub-5 nm nodes [36].

Ultimately, PEALD benchmarks higher in etch resistance, thickness uniformity, and interface stability than legacy techniques. These metrics are becoming increasingly vital as node scaling pushes structural dimensions and electrical tolerances to atomic limits [37].

8.2. CMOS Compatibility, Throughput, and Cost Considerations

Despite their advantages, widespread adoption of PEALD ESLs hinges on practical considerations including CMOS compatibility, tool throughput, and cost-efficiency. From a front-end-of-line (FEOL) perspective, ESL materials such as SiN_x and Al_2O_3 deposited via PEALD show excellent process modularity and compatibility with existing HKMG stacks, thermal anneals, and S/D activation conditions [38].

However, throughput remains a bottleneck. Traditional PEALD cycles take significantly longer than high-density plasma CVD or spin-on alternatives due to sequential pulsing and purging requirements. Although batch PEALD reactors and spatial ALD techniques have emerged to address this, integration with high-volume manufacturing still requires careful tool matching and chamber optimization [39].

Cost-wise, PEALD systems involve higher capital expenditure and precursor consumption, particularly when using metal-organic or halide-based compounds with short shelf lives. Process engineers mitigate this by optimizing pulse durations, reducing overexposure, and recycling chamber flows without sacrificing deposition quality [40].

Integration complexity also factors into cost. PEALD ESLs must align with multiple patterning and alignment steps, requiring tight overlay control and plasma uniformity. Any deviation can lead to alignment drift or fin bending, triggering yield loss.

Despite these constraints, the value proposition of PEALD ESLs remains strong due to their unparalleled conformality and reliability performance. In nodes below 5 nm, where etch profile fidelity and leakage suppression dominate yield metrics, PEALD-based ESLs may become indispensable—even if they incur a marginal cost premium [41].

Foundries are already co-optimizing ESL flows with contact and gate module stacks to minimize integration friction while maintaining CMOS electrical compliance. This trend will likely continue as ESL performance is seen not just as an integration requirement but a strategic reliability enabler [42].

8.3. Scalability toward Gate-All-Around (GAA) and Nanosheet FETs

As the industry transitions from FinFET to Gate-All-Around (GAA) and nanosheet FETs, the performance requirements for etch-stop layers become more stringent. GAA architectures introduce complex 3D nanowire and nanosheet topographies, where even minor non-uniformities in ESL thickness can impact gate control, channel stress, and parasitic capacitance [43].

PEALD is uniquely positioned to meet these challenges due to its angstrom-level thickness precision and trench-filling capability. In nanosheet FETs, conformal ESLs are required between stacked nanosheets to isolate vertical gates and prevent leakage between layers. Spin-on and thermal CVD techniques cannot deliver sufficient uniformity at this scale [44].

Moreover, GAA scaling requires selective ESL deposition without compromising epitaxial growth regions or sacrificial oxide removal steps. This makes plasma-assisted ALD attractive, as it can be tuned to deposit selectively via surface energy modulation and in situ precursor chemistry [45].

The scalability of PEALD ESLs toward GAA nodes also depends on low-temperature process viability (sub-400°C), enabling co-fabrication with temperature-sensitive layers such as strain liners or doped epi-regions [46].

In summary, as device geometries transition into vertically stacked, atomically narrow channels, PEALD etch-stop solutions offer the best path forward in ensuring uniformity, isolation, and long-term reliability in next-generation CMOS logic platforms [47].

9. Conclusions and Future Outlook

9.1. Summary of Key Findings and Contributions

This article provides a comprehensive analysis of conformal etch-stop layers (ESLs) in advanced FinFET fabrication, with a focus on materials, deposition techniques, integration challenges, and reliability outcomes. As semiconductor nodes scale below 5 nm, the need for precision in patterning and protection becomes paramount. ESLs serve as essential components in defining etch boundaries, minimizing gate leakage, preserving interface quality, and ensuring dimensional stability across high-aspect-ratio features.

The investigation highlights plasma-enhanced atomic layer deposition (PEALD) as a dominant technique due to its superior conformality, low-temperature processing, and process tunability. Compared to thermal ALD or spin-on approaches, PEALD offers better uniformity and tighter integration with complex 3D device geometries. Reliability testing shows that PEALD ESLs outperform conventional methods in suppressing gate leakage, enhancing time-dependent dielectric breakdown (TDDB) performance, and resisting plasma-induced damage.

Additionally, the analysis covers the critical material properties—such as dielectric constant, hydrogen content, and bond strength—that influence ESL performance. Process control strategies, including precursor pulse tuning and remote plasma configurations, are emphasized for minimizing variability and optimizing growth per cycle. Integration with gate, spacer, and source/drain modules is explored in detail, along with emerging challenges in nanosheet and GAA architectures.

Overall, this study contributes a foundational framework for understanding and optimizing ESLs in FinFET nodes and beyond.

9.2. Strategic Implications for Sub-3 nm Node Technology Roadmap

As the industry targets sub-3 nm nodes and approaches fundamental physical scaling limits, strategic materials and process integration decisions will determine the viability of each technology generation. Etch-stop layers are transitioning from passive boundary markers to critical enablers of pattern fidelity, leakage suppression, and electrical stability. Their integration must now support extreme aspect ratios, atomic-scale gate dimensions, and multi-stack channel configurations.

The findings in this work underscore the need for ESL materials that are not only chemically robust but also integration-friendly and CMOS-compatible. The shift from FinFET to GAA requires ESLs capable of high selectivity, ultrathin conformality, and minimal dielectric loss. Thermal budget constraints in advanced logic processes further necessitate deposition methods that operate below 400°C, making PEALD-based solutions increasingly attractive.

From a roadmap perspective, ESLs are expected to contribute to yield enhancement through more precise etch control, improved line-edge definition, and reduced defectivity during critical pattern transfer steps. Their interaction with high-k dielectrics and metal gates also influences Vt tuning strategies and reliability scaling. Therefore, material design must be co-optimized with device electrical targets and back-end integration flows.

Moreover, as new logic architectures like complementary FETs (CFETs) emerge, vertical stacking will require ESLs to perform in dual-function roles—acting as both diffusion barriers and selective patterning agents. The trajectory of sub-3 nm nodes clearly places ESLs at the heart of patterning control and device protection, necessitating continuous innovation and cross-disciplinary collaboration across material science, plasma physics, and process engineering.

9.3. Future Research Directions: Plasma Chemistry Design and AI-Based Process Control

Looking forward, the development of next-generation etch-stop layers will rely heavily on innovations in plasma chemistry and AI-assisted process control. One promising direction involves engineering plasma chemistries with tailored radical and ion profiles to modulate film growth kinetics, density, and etch selectivity. Mixed gas plasma environments, such as H_2/NH_3 or Ar/O_2 combinations, allow for tunable surface reactivity, enabling finer control over film composition and interface properties.

Another research frontier is the exploration of heterostructured or hybrid ESLs, where alternating layers or doping agents introduce functional gradients in the film. These multilayered structures could offer superior resistance to plasma damage while maintaining desirable electrical characteristics. Material systems such as B_xC_Y or doped SiN_x variants show potential in balancing conformality, thermal stability, and mechanical resilience.

Artificial intelligence and machine learning will play a transformative role in optimizing ESL deposition. Closed-loop systems equipped with in situ sensors—such as quartz crystal microbalance (QCM), ellipsometry, or mass spectrometry—can feed real-time process data into predictive models. These AI frameworks will enable on-the-fly adjustments to precursor flow, plasma power, or substrate bias, ensuring consistent film quality even in complex 3D structures.

Moreover, digital twins of deposition chambers may allow engineers to simulate process-structure-property relationships with high fidelity before physical trials. These models can reduce development time, improve yield ramp-up, and accelerate material discovery for ESLs. As device dimensions shrink and integration density rises, the demand for smarter, adaptive process systems will only intensify.

In essence, the future of ESL development will be defined by a fusion of advanced plasma science and intelligent automation—bridging the gap between atomic-scale engineering and scalable, defect-free manufacturing

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