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Design of low-power CMOS VLSI circuits using multi-objective optimization in genetic algorithms

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Abstract

This paper presents a design CAD tool for automated design of digital CMOS VLSI circuits. In order to fit the circuit performance into desired specifications, a multi-objective optimization approach based on genetic algorithms (GA) is proposed and the transistor sizes are calculated based on the analytical equations describing the behavior of the circuit. The optimization algorithm is developed in MATLAB and the performance of the designed circuit is verified using HSPICE simulations based on 0.18µm CMOS technology parameters. Different digital integrated circuits were successfully designed and verified using the proposed design tool. It is also shown in this paper that, the design results obtained from the proposed algorithm in MATLAB, have a very good agreement with the obtained circuit simulation results in HSPICE.

Keywords: VLSI; Genetic algorithm; Full-Adder; CMOS; Low-Power; Optimization

1. Introduction

With the increasing demand for digital integrated circuits, the optimal design of VLSI circuits such as high-performance Full-Adders is becoming more challenging and time consuming. The performance of a high-performance digital integrated circuit such as full-adder, is characterized by a number of performance measures such as power dissipation, propagation delay, power-delay product (PDP) and layout area which are considered as the main objectives that are required to be optimized simultaneously [1].

The performance measures of a digital integrated circuit are usually determined by the design parameters such as passive component values such as load capacitance C_L, bias voltages and currents and transistor dimensions (W, L) [2]. However, the performance of a digital integrated circuit is very sensitive to the values of the design parameters. So, the problem of designing an optimized digital integrated circuit is to determine the values of design parameters in order to optimize an objective measure while satisfying constraints on the other performance measures.

Since, some performance parameters of digital integrated circuits are most likely conflicting with each other, optimized digital IC circuit design suffers from long design time, high complexity, high cost and requires highly skilled designers. Furthermore, finding an optimal solution for design of digital integrated circuits is very challenging and time consuming. Therefore, developing reliable tools for automated design of widely used digital integrated circuits such as full-adder circuits is very important [1, 2].

Soft computing methods can be used to decrease the design duration and time-to-market of VLSI circuits [3, 8]. One of those methods called Genetic Algorithm (GA) is a global search algorithm which models the process of natural evolution in order to optimize the main objective of a design problem. This algorithm can be successfully applied to a class of

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optimization problems such as digital circuit design problem, where the search space is too large to converge by classic and conventional techniques and also it can save much time in finding the design target [4].

In this paper, an automated design algorithm is proposed which achieves the performance measures for a particular application and then the selected circuit topology is designed and the transistors are automated sized and the width and length of all transistors are calculated.

The sizing of transistors usually requires several iterations, trial and error process should be done by the computer simulations and soft computing methods such as GA can be used to decrease the design time. In this paper, a CMOS widely used full-adder circuit is designed and optimized using multi-objective optimization approach implemented in MATLAB using GA as a multi-objective optimization tool. HSPICE software is also used as a verification tool for circuit simulations. Figure 1, shows the full-adder circuit structure considered for design optimization in this paper.

This paper is organized as follows:

In section II, a brief review of the genetic algorithm as an optimization tool is presented. The proposed design algorithm for automated design of a full-adder circuit is presented in section III. In section IV, the simulation results are provided where the performance of the proposed design and optimization approach is compared with other reported designs to verify the benefits of the proposed approach over previously reported designs. Finally, concluding remarks are presented in section V.

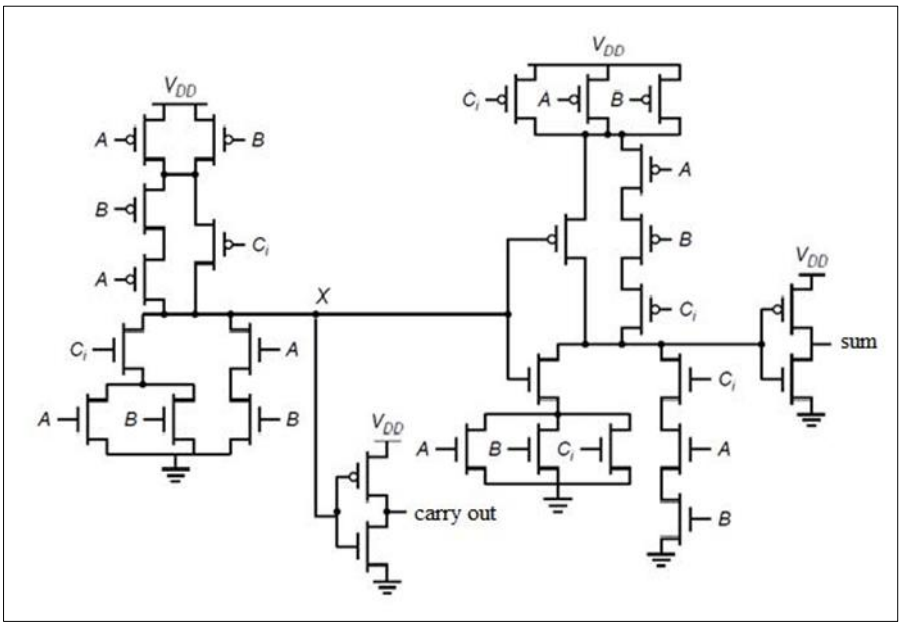

Figure 1 CMOS full-adder Circuit structure considered for design and optimization in this paper [1]

2. Brief Review of Genetic Algorithm (GA)

Genetic algorithm (GA) is a soft computing technique inspired by the principles of natural evolution. GA is an optimization technique, which starts with a set of initial solutions, also called initial population, randomly generated. In GA, each unknown parameter is called gene and the vector of unknown parameters is called chromosome [4]. Also, there is a fitness function (ff) that is considered as a criterion for evaluating the genetic algorithm (GA) operation and performance. There is an operator called crossover which mixes the initial population and allows GA to exploit the set of current solutions (individuals) in order to obtain better solutions in comparison with those of previously set. Similar to the biological evolution, GA uses mutation operator which causes a randomly minor change in individuals and allows GA to explore the full space of possible solutions to the design problem.

When the steps of selection, crossover and mutation are done, a new population is resulted and a new set of solutions is generated. This algorithm is repeated several times and in every new generation all the individuals are evaluated, and the best solutions found based on the best fitness are ranked.

However, the purpose of the GA is to determine the elements of the unknown vector (chromosome) to maximize the value of the defined fitness function. In each generation, new population of chromosomes is enhanced in fitness function by means of some operators such as cross over and mutation. Finally, GA needs a halt (terminating) condition in order to end the generation process of new solutions (individuals). If there is not any sufficient improvement in two or more consecutive generations, the genetic algorithm process can be stopped. In other cases, a time limitation can be used as a criterion for ending the process or a desired fitness value within some percentage of accuracy can be considered as the halt condition [4].

3. Proposed design method

As mentioned above, full-adders are one of the most important building blocks of computational circuits and systems. As it is discussed before, all the performance parameters of a full-adder circuit, are determined by the dimensions of the transistors W, L (with and length of the transistor) as well as the passive component values such as load capacitance C_L.

In order to fit the circuit performance parameters into desired specifications, a multi-objective optimization approach based on genetic algorithms (GA) is proposed and the transistor sizes are calculated based on the power and delay analytical equations describing the behavior of the full-adder circuit. The optimization algorithm is developed and implemented in MATLAB while the performance of the designed circuit is verified using HSPICE simulations based on 0.18µm CMOS technology parameters.

The multi-objective GA is used in this paper to optimize the performance measures such as: power consumption, delay and PDP parameter for the full-adder circuit shown in figure 1. The first step to solve the design and optimization problem is to find the proper analytical equations describing the behavior of the circuit. In this step, the knowledge of an expert digital integrated circuit designer is formulated in the form of analytical power and delay equations. Then, unknown design parameters in analytical equations are considered as a vector of design variables which forms the chromosome that should be solved using GA.

The chromosome contains transistor dimensions W, L and of transistors. Of course, some of the widths and lengths for the transistors that have similar role in the full-adder circuit topology are equal. The automated design and optimization algorithm is coded in MATLAB using the analytical equations the full-adder shown in figure 1.

In this section, the analytical delay and power consumption equations of the full-adder presented in figure1, are presented based on the method discussed in [2, 5]. As it is discussed in [2,5], the propagation delay of a digital integrated circuit is mainly dependent on the internal time constants "τ" which are formed from the internal parasitic resistances and capacitances of the transistors as well as the load capacitance. Therefore, in order to calculate the propagation delay, the digital switching circuit model which models the parasitic resistances and capacitances of the circuit should be considered [7]. In the next step, based on the resulted switching circuit model the analytical equations for the propagation delay can be extracted. Figure 2 and 3, show the switching circuit model of the full-adder for both the "SUM" and "Carry-out" outputs.

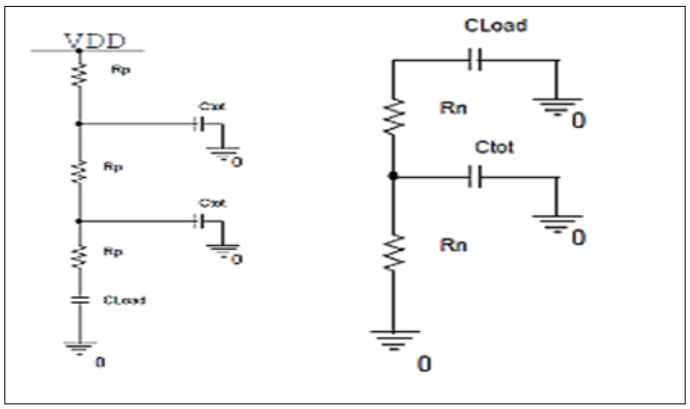

Figure 2 Delay circuit model for Carry-out output

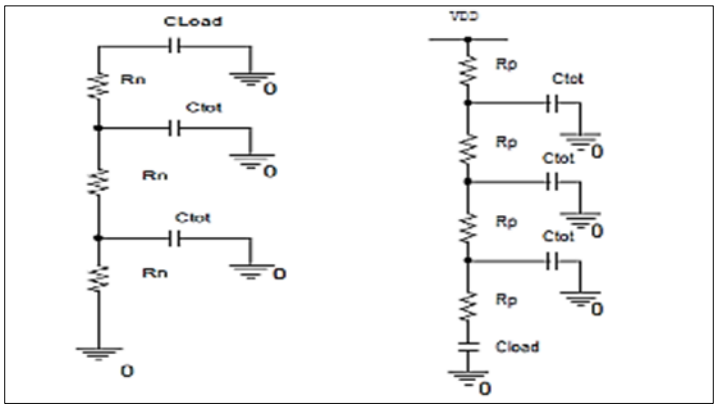

Figure 3 Delay circuit model for SUM output

So, from figure 2, the total time constant of the pull-up T_p and pull-down T_N sections of the Carry out circuit can be expressed as:

$$T_P = R_P * C_{TOT} + 2 * R_p * C_{TOT} + 3R_P * C_{LOAD} \quad (1)$$

$$T_N = (R_N + R_N)C_{LOAD} + R_N * C_{TOT} \quad (2)$$

In addition, the high-low and low-high propagation delay for the Carry out signal can be expressed as:

$$T_{PHL} = 0.69 * \left(\left(3 * R_{SP} * \left(\frac{L}{W_P}\right) * 5 * C_{OX}\right) + \left(6 * R_{SP} * \left(\frac{L}{W_P}\right) * C_L\right)\right) \quad (3)$$

$$T_{PLH} = 0.69 * \left(\left(1 * R_{SN} * \left(\frac{L}{W_N}\right) * 5 * C_{OX}\right) + \left(3 * R_{SN} * \left(\frac{L}{W_N}\right) * C_L\right)\right) \quad (4)$$

Where, C_{tot} is the total effective capacitance seen at the output node, Cox is the oxide capacitance per unit area, R_{sp}, R_{sn} are the sheet resistance of the PMOS and NMOS transistors with minimum area and W_N, W_P are the width of the NMOS and PMOS, respectively.

On the other hand, from figure 3, the total time constant of the pull-up T_p and pull-down T_N sections of the SUM circuit can be expressed as:

$$T_P = R_P * C_{TOT} + 2 * R_P * C_{TOT} + 3 * R_P * C_{TOT} + 4 * R_P * C_{LOAD} \quad (5)$$

$$T_N = 2 * R_N * C_{TOT} + R_N * C_{TOT} + 2 * R_N * C_{LOAD} \quad (6)$$

In addition, the high-low and low-high propagation delay for the Sum output signal can be expressed as:

$$T_{PHL} = 0.69 * \left(\left(3 * R_{SP} * \left(\frac{L}{W_P}\right) * 5 * C_{OX}\right) + \left(6 * R_{SP} * \left(\frac{L}{W_P}\right) * C_L\right)\right) \quad (7)$$

$$T_{PLH} = 0.69 * \left(\left(3 * R_{SN} * \left(\frac{L}{W_N}\right) * 5 * C_{OX}\right) + \left(6 * R_{SN} * \left(\frac{L}{W_N}\right) * C_L\right)\right) \quad (8)$$

As it is obvious from the circuit topology and the switching circuit models, some widths and lengths are considered as equal, so, the unknown design parameters such as transistor dimensions W_N, W_P, L, etc. can be considered as the chromosome vector which is titled as the design variables that can be solved by the optimization algorithm.

For the full-adder circuit structure of figure 1, it is assumed that, V_{DD}= 1V, V_{SS}=0V and CL=0.1pF. The GA program determines this vector of the parameters such that the fitness function is maximized. Fitness is a numerical quantity describing how well a solution (individual) meets predefined design objectives and constraints. On the other hand, the

total performance of a circuit is evaluated by fitness function. For fitness evaluation in a multi-objective problem, several methods can be used. Here, the fitness function (*ff*) is defined as [4, 10]:

$$ff = \sum_{i=1}^{n} Wi * fi \quad (9)$$

fi = desired value for objective i
wi = weight coefficient of objective i
n = number of objectives

A multi-objective problem can be solved by combining the objectives (f_i), into one numerical quantity whose solution is so-called "Pareto optimal point". It can be shown that this combined function is Pareto optimal. It is up to designer to choose the appropriate weight coefficients W_i. Each set of weights generates one Pareto point. Thus, by varying the weights and solving the problem a Pareto surface, formed by a set of Pareto points, can be created. Then, the pre-defined search algorithm can find the optimum solution and the obtained chromosome is resulted from the optimization algorithm.

4. Simulation results

In order to verify the performance of the proposed method, the full-adder circuit shown in figure 1, is successfully designed and optimized for the desired performance values summarized in table1, using the optimization method discussed above. Figure 4, shows the full-adder circuit design and transistor sizing optimization process employed in this paper. The automatic design algorithm and multi-objective optimization using genetic algorithm, is performed and coded in MATLAB. The proposed algorithm calculates the best dimensions of transistors (W, L), that generate the best fitness function value. HSPICE circuit simulations using 0.18μm CMOS technology parameters, are carried out using the obtained design parameters resulted from MATLAB in order to verify the performance of the design algorithm.

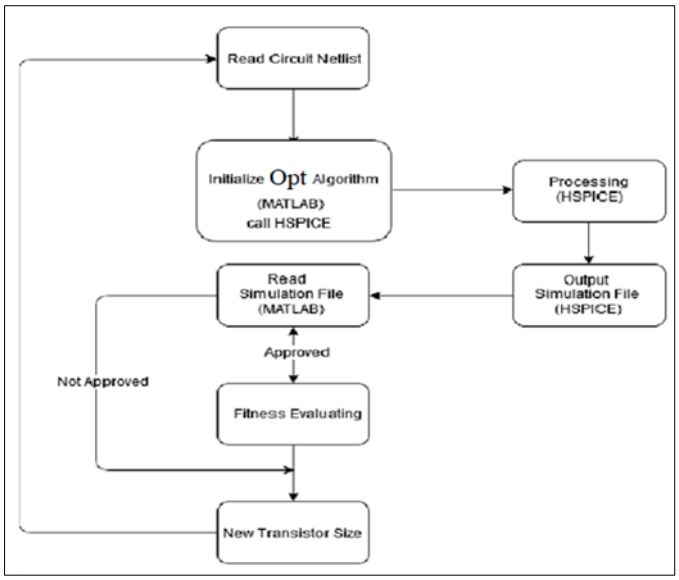

Figure 4 Flowchart of the automatic full-adder circuit design and optimization process

As it is obvious in figure 4, the design variables (transistor dimensions W, L) resulted from the optimization algorithm in MATLAB, are used for HSPICE circuit simulations in order to verify the performance of the full adder circuit.

In a multi-objective optimization problem, such as the full-adder circuit design, different and sometimes conflicting objective functions such as power consumption and propagation delay must be optimized simultaneously [8, 10, 11]. One solution to such optimization problems with multiple objective functions is to combine the values resulted for each objective with different weights (W_i) to obtain a proper fitness value. In this approach, the multi-objective problem converts to a single-objective optimization problem, but to use this method properly, the values of the weights should be selected by the designer. Another approach is to obtain a set of solutions that can optimize the maximum possible number of objective functions. This set of the optimal solutions titled as "Pareto". Firstly, the initial values for W_N, W_P are randomly selected and the performance parameters (objectives) of propagation delay and power consumption are

calculated regarding the mentioned analytical equations. Then, two separate functions in the Pareto front for propagation delay and power consumption should be defined. These two functions have two variables Wn and Wp, which were initially calculated through the fitness function. The resulting values of Wn and Wp are then replaced into two functions. Finally, with the calculations performed on each Pareto, the optimal values for different objectives can be shown in one Pareto front together.

Table 1 Desired performance values for simulations

Performance Parameter	Constraints
Power	<500 µW
delay	<400 ps
Vdd	1V
Vss	0
Wmax	36µm
Wmin	0.18µm
L	0.18µm
CL	0.1pF

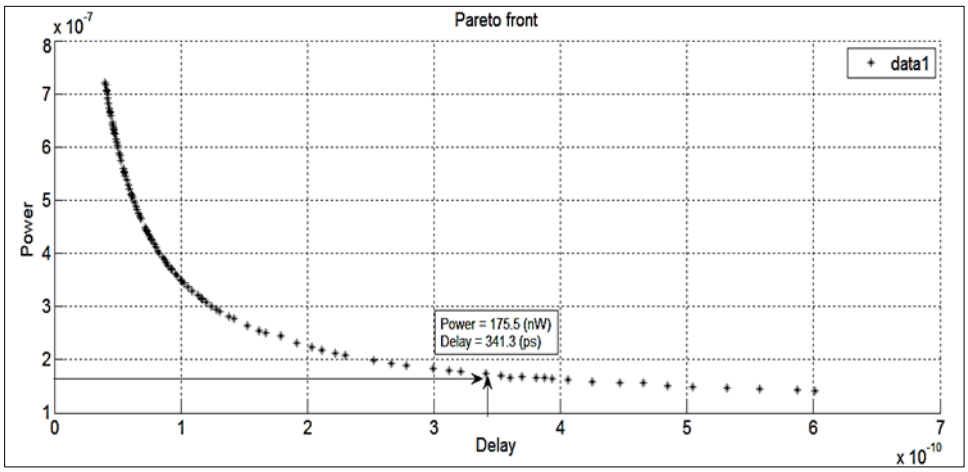

Figure 5 Simulation results for the power performance of the SUM circuit

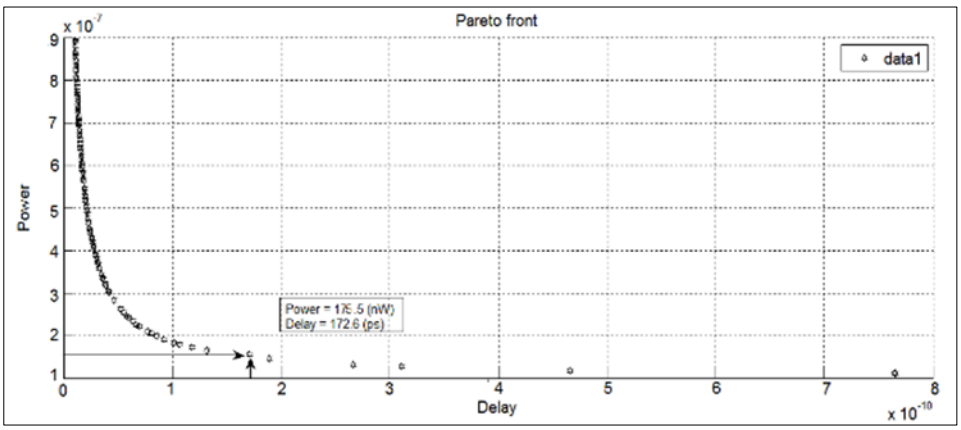

Figure 6 Simulation results for the power performance of the Carry circuit

As it is obvious in figures 5, 6, different circuit simulations were successfully performed and the two objectives of power consumption and propagation delay for both SUM and Carry circuits are calculated and verified using the proposed design tool. So, regarding the constraints of the optimization problem summarized in table 1, the minimum power consumption of the SUM and Carry circuits is obtained as 175.5nW, while their corresponding delay values in this "low-power" Pareto are obtained as 343.1ps and 172.6ps, respectively.

On the other hand, from the "high-speed" point of view which demands the minimum propagation delay value for the full-adder circuit, a "high-speed" Pareto can be considered in which the minimum delay value can be resulted at an increased value of power consumption. Figure 7, shows the obtained Pareto for low-delay performance.

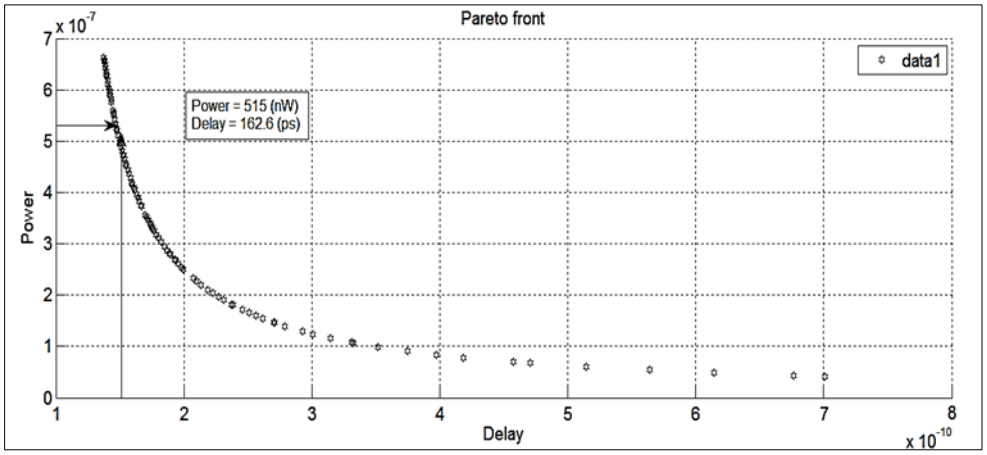

Figure 7 Simulation results for the delay performance of the full-adder circuit

As it is obvious in figure 7, the minimum propagation delay of the circuit is obtained as 162.6ps, while its corresponding power consumption value in this Pareto is obtained as 515nW.

Table 2, summarizes the designed full-adder circuit performances for two different design scenarios of "low-power" scenario that represents the minimum power consumption and "high-speed" scenario which represents the minimum propagation delay.

Table 2 Simulation results of the full-adder using the proposed transistor sizing optimization approach

Low-power				**High-Speed**		
PDP (aJ)		**Delay**	**Power(nW)**	**PDP (aJ)**	**Delay(ps)**	**Power(nW)**
SUM	59.9	341.3	175.5	83.7	162.6	515
CARRY	30.3	172.6	175.5	52.7	102.4	515

It is also observed that, the circuit performance parameters obtained from the proposed design algorithm in MATLAB, have very good agreement with the obtained circuit simulation results in HSPICE which indicates the good design accuracy for the proposed transistor sizing approach.

Figures 8, 9, show the transient simulation results for both the full-adder output signals of "SUM" and "Carry out" with respect the input signals A, B and C.

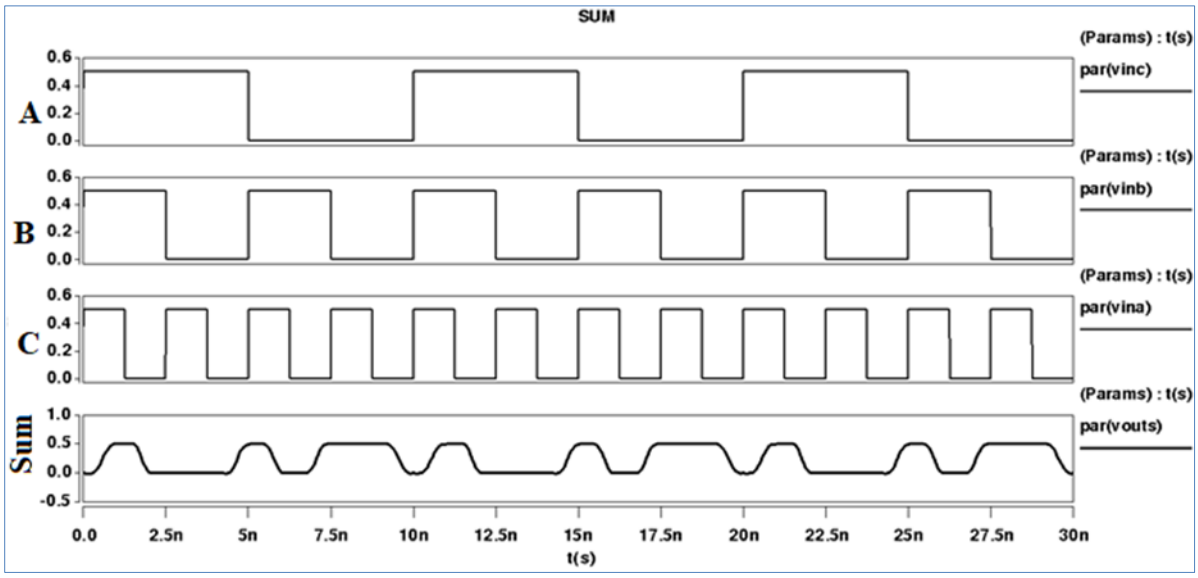

Figure 8 Transient simulation result of designed full adder for "SUM" output

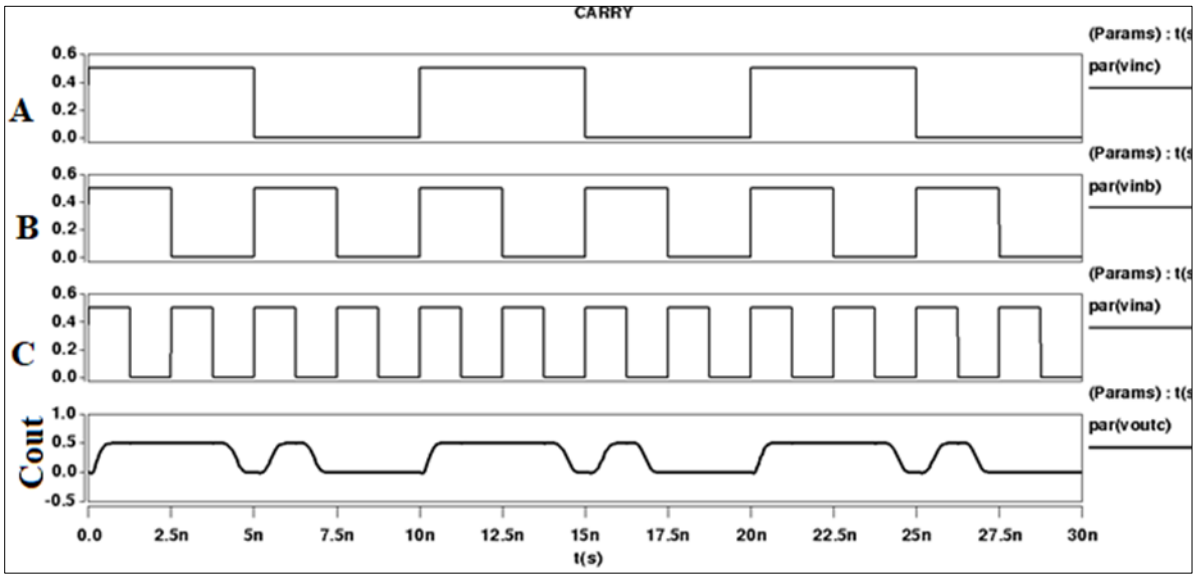

Figure 9 Transient simulation result of designed full adder for "Carry out" output

Furthermore, in order to investigate the benefits of the proposed design approach over the other reported designs, the circuit performance parameters of the designed full-adder circuit are compared with other reported designs and summarized in table 3.

As it is obvious in table 3, the proposed design approach not only reduced the power consumption of the circuit effectively, but also due to the use of an evolutionary optimization algorithm in the transistor sizing process, the optimized transistor sizes are selected in a way that results in a reduced chip size area.

However, due to the fact that, the internal parasitic capacitances and resistances mainly cooperate in the transient performance of the circuit such as the switching speed limitations as well as the dynamic power consumption, so, by employing the proposed design and transistor sizing optimization approach, not only the power consumption but also the propagation delay of the full-adder circuit reduced significantly which resulted in a considerable reduction of the power-delay product PDP performance of the circuit in comparison with other previously reported designs. It is also justified that, the proposed design and optimization approach enables the designer to successfully design a VLSI digital

integrated circuit for the required circuit performances in all the low power consumption, low propagation delay and power-efficiency (low-PDP) scenarios by setting different design constrains in the proposed transistor sizing and optimization algorithm.

Table 3 Performance comparison with other reported designs

	[6]	[11]	[9]		This work (low-power)	
Performance	**Full-Adder**	**Full-Adder**	**SUM**	**CARRY**	**SUM**	**CARRY**
Power	376.18 (E-4)	13.4 (E-6)	695.4 (E-9)	695.4 (E-9)	175.5 (E-9)	175.5 (E-9)
Delay	244.92 (E-12)	16.1 (E-12)	176.9 (E-12)	107.1 (E-12)	341.3 (E-12)	172.6 (E-12)
PDP	921.34 (E-14)	215.74 (E-18)	122 (E-18)	74 (E-18)	59.9 (E-18)	30.3 (E-18)

5. Conclusion

In this paper, a new transistor sizing optimization approach for automated design of digital integrated circuits using multi-objective genetic optimization algorithm based on the circuit's behavioural equations is presented. The analytical equations and circuit simulations were combined to generate an accurate design and optimization tool for digital integrated circuits design. The proposed design algorithm can optimize the transistor sizes in order to meet the design objectives. In order to verify the performance of the proposed algorithm, a CMOS full-adder circuit was successfully designed and simulated in MATLAB and HSPICE using 0.18 µm CMOS technology model parameters. As it is shown in this paper, the proposed transistor sizing algorithm not only reduces the power consumption of the full-adder circuit but also, by optimizing the transistor dimensions which reduces the internal parasitic capacitances and resistances of the circuit, the propagation delay and PDP performances of the full-adder circuit are improved effectively. Finally, the digital integrated circuit designers can benefit from the proposed approach discussed in this paper, to design the high-performance VLSI circuits in the future coming fabrication technologies.

Compliance with ethical standards

Disclosure of conflict of interest

No conflict of interest statement.

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